Application Note

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Trenz TEBF0808 + TE0808-04-6EB21A SoM with Analog Devices AD-FMCDAQ2-EBZ Evaluation Board

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Revision history

Rev.	Date	Author	Description
0	11. 22. 2019	L. Kohout	Initial version of the document
1			
2			

Content

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1 Introduction

This document is a quick guide describing steps to run a basic demo on Trenz Electronic TEBF0808 carrier board [1] with Trenz Electronic TE0808-04-6EB21A System on Module [2] and with Analog Devices AD-FMCDAQ2-EBZ evaluation board [3]. The procedure has been tested on PC running Ubuntu 16.04 LTS and Windows 7.

2 Used tools and Resources

- Trenz Electronic TEBF0808 carrier board [1].
- Trenz Electronic TE0808-04-6EB21A SoM. It contains Xilinx Zynq UltraScale+ device with 4GB DDR4 memory [2].
- Analog Devices AD-FMCDAQ2-EBZ evaluation board [3]. Be careful during the FMC board installation, some components are too close to distance columns and they can be easily damaged. It is recommended to use distance columns enclosed with the board.
- Mini USB cable.
- 50 Ohm coaxial cable with SMA connectors – 2x.
- Xilinx Software Development Kit 2018.2, it a part of Xilinx Vivado Design Suite 2018.2 (Web Pack edition is sufficient). To download the tool go to Xilinx web page: https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html.

3 Demonstrator Startup

To run the demonstrator follow the steps bellow.

1. Unpack the package attached with this application note. The package content is listed in Section 4.
2. Start Xilinx SDK 2018.2, set workspace to *prebuilt/te0808-6EG-1EE/sdk*.
3. Create new HW project, menu
   File->New->Project...
   Xilinx->Hardware Platform Specification
   Project name: *hw*
   Browse to file *prebuilt/te0808-6EG-1EE/system.hdf*
4. Create Board Support Package, menu
   File->New->Board Support Package
   Project name: *bsp*
   Hardware Platform: *hw*
   CPU: *psu_cortex53_0*
   Compiler: *64-bit*
   Board Support Package OS: *standalone*
5. Import SW project, menu
   File->Import
   General->Existing Projects into Workspace
   Click *Browse* button
   Click *OK* button
   Select project: *sw*
   Click *Finish*
6. Compile the project, menu *Project->Build All*.

7. As this demonstrator has been developed from the demonstrator for Xilinx XCU102 board, initial configuration of the Zynq UltraScale+ has to be modified. Patch *psu_init.tcl* file:

   Replace file *prebuilt/te0808-6EG-1EE/sdk/hw/psu_init.tcl*

   with *prebuilt/te0808-6EG-1EE/psu_init.tcl* file.

   It is possible that this step will be required after each Xilinx SDK startup, because the file is auto-generated.
8. Connect mini USB cable to JTAG, XMOD1 module on the TEBF0808 carrier board.
9. On the AD-FMCDAQ2-EBZ board, connect OUT_A with IN_A and OUT_B with IN_B. Use 50 Ohm coaxial cables with SMA connectors.
10. Configure TEBF0808 carrier board
    - Set *S4* to "off off off on"
    - Set *S5* to "on on on on"
    - All other switches and jumpers let in their defaults.
11. Power the board on. Push button S1 and then push button S2.
12. Start serial terminal, putty for instance. The settings are:
    - Baud rate – 115200
    - Data bits – 8
    - Stop bits – 1
    - Parity – none
    - Flow control – none

    Download bitstream to the board, in Xilinx SDK *Xilinx->Program FPGA*
13. Download SW to the board, in *Project Expolorer* select *sw*, right click on it:

    Run As->Launch on Hardware (System Debugger)
14. Observe the serial terminal:

```
Xilinx Zynq MP First Stage Boot Loader
Release 2018.2   Nov 22 2019  -  09:59:17
PMU-FW is not running, certain applications may not be supported.
Available sampling rates:
        1 - ADC 1000 MSPS; DAC 1000 MSPS
        2 - ADC  500 MSPS; DAC 1000 MSPS
        3 - ADC  500 MSPS; DAC  500 MSPS
        4 - ADC  600 MSPS; DAC  600 MSPS
        5 - ADC 1000 MSPS; DAC 2000 MSPS (2x interpolation)
choose an option [default 1]:
1 - ADC 1000 MSPS; DAC 1000 MSPS
Tx link is enabled
Measured Link Clock: 250 MHz
Link status: DATA
SYSREF captured: Yes
Rx link is enabled
Measured Link Clock: 250 MHz
Link status: DATA
SYSREF captured: Yes
adc_setup adc core initialized (1000 MHz).
dac_setup dac core initialized (1000 MHz).
daq2: setup and configuration is done
daq2: RX capture done.
```

    The application also prints captured data (sin wave). Complete set of the used hardware that can run the demonstrator is shown in Figure 1.

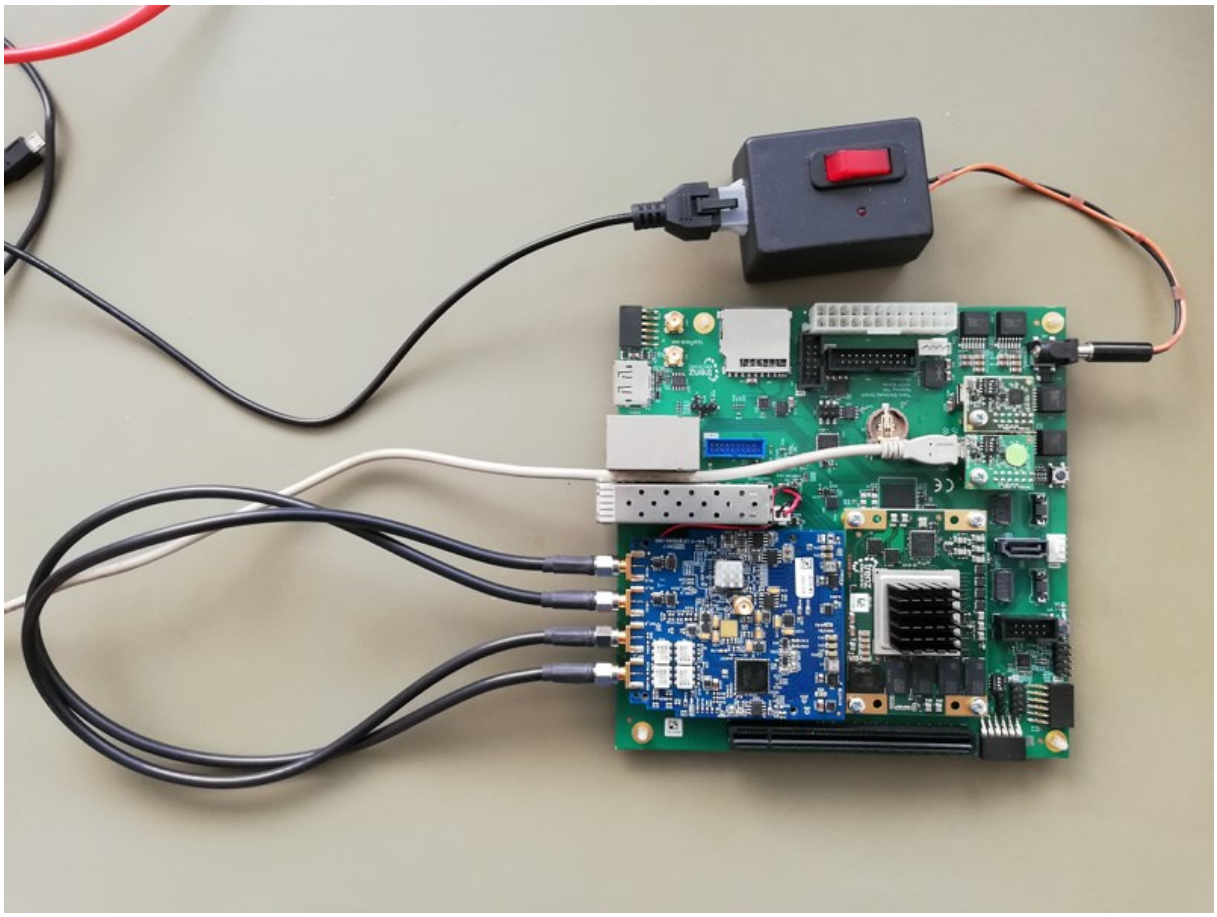

Figure 1: Complete HW set of the demonstrator.

4 Package Content

```
.
├── doc
├── sdk
├── BOOT.bin
├── psu_init.tcl
├── sw.elf
└── system.hdf
```

5 References

[1] Trenz Electronic, „UltraITX+ Baseboard for Trenz Electronic TE080X UltraSOM+," [Online]. Available: https://shop.trenz-electronic.de/en/TEBF0808-04A-UltraITX-Baseboard-for-Trenz-Electronic-TE080X-UltraSOM.

[2] Trenz Electronic, „UltraSOM+ MPSoC Module with Zynq UltraScale+ XCZU6EG-1FFVC900E, 4 GB DDR4," [Online]. Available: https://shop.trenz-electronic.de/en/TE0808-04-6BE21-A-UltraSOM-MPSoC-Modul-with-Zynq-UltraScale-XCZU6EG-1FFVC900E-4-GB-DDR4.

[3] Analog Devices, „AD-FMCDAQ2-EBZ Evaluation Board," [Online]. Available: https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad-fmcdaq2-ebz.html#eb-overview.

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