





Python 1300 Video Sensor Evaluation Platform for TE0720-03-2IF SoM on TE0701-05 Carrier

Jiří Kadlec, Zdeněk Pohl, Lukáš Kohout <u>kadlec@utia.cas.cz</u>, <u>xpohl@utia.cas.cz</u>, <u>kohoutl@utia.cas.cz</u> phone: +420 2 6605 2216 UTIA AV CR, v.v.i.

Revision history:

Rev.	Date	Author	Description
1	05.07.2016	Jiří Kadlec	Evaluation package for Xilinx SDK 2015.4
2	18.07.2016	Jiří Kadlec	SD cards with compiled SDSoC SW projects

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1. Summary

1.1 Key features

This application note describes HW platform performing edge detection and motion detection video processing for ON Semi Python 1300 colour video sensor with fixed resolution (1280x1024p60).

Arm Cortex A9 processor of Xilinx Zynq is performing initialisation and synchronisation of the video processing chain. Program and the FPGA image is downloaded to the board from the Xilinx SDK 2015.4 via USB JTAG to the 1GB DDR3 located on the Zynq system on module. System can be also started directly from the SD card. Arm processor initiates the IP cores in the programmable logic (PL) part of the Zynq. It also initiates the Python 1300 video sensor and the HDMI video output to monitor with fixed resolution 1280x1024p60.

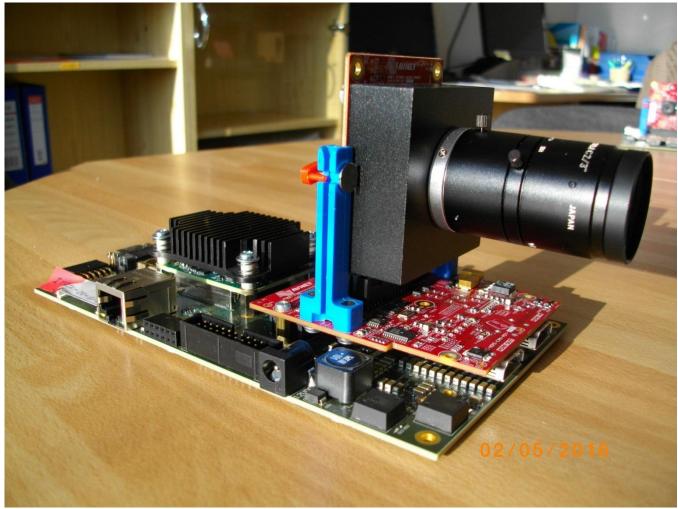


Figure 1: Python 1300 video sensor evaluation platform.

- Raw video data are provided by the Python 1300 video sensor.
- Data are processed into the YCrCb 16 bit per pixel format and stored by Video DMA (VDMA) to input video frame buffers (VFBs) defined in the DDR3.
- HW DMA controller(s) send data from the input VFBs to the processing accelerators in PL.
- Another DMA controller(s) send processed data from HW to the output VFBs in DDR3.
- Second part of the VDMA is sending data to the HDMI display with resolution 1280x1024p60.

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signal processing



1.2 Project sh01: Edge detection with single HW accelerator

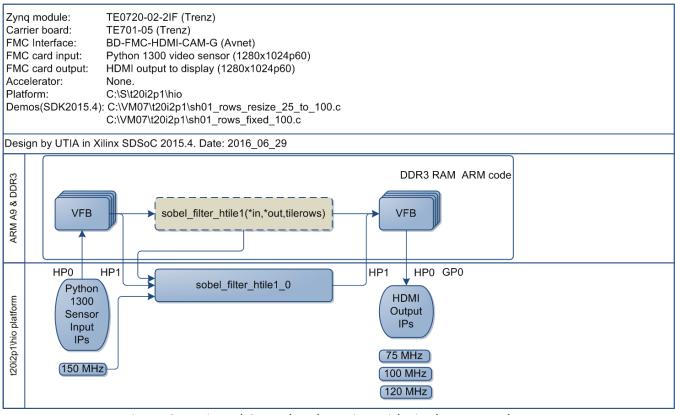


Figure 2: Project sh01 - Edge detection with single HW accelerator

te0701-05 te0720-2i: FPS

36,82

80

80

40

10,73

TE0720-02-2IF Sobel 1x

Energy per one frame (SW): 558.06.3 mJ Energy per one frame (HW): 162.63 mJ Energy per frame reduction: 3.43 x

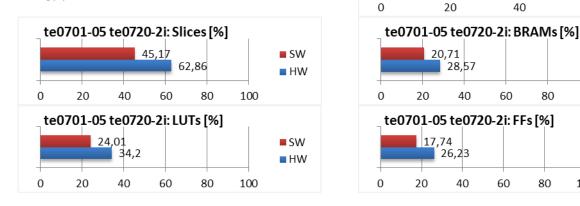


Figure 3: Project sh01 - Energy per frame reduction and used HW resources.



SW

HW

SW

HW

SW

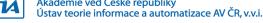
HW

60

100

100

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1.3 Project sh02: Edge detection with two HW accelerators

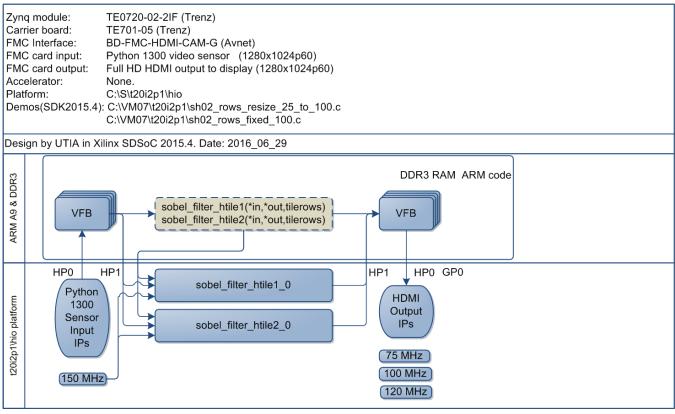
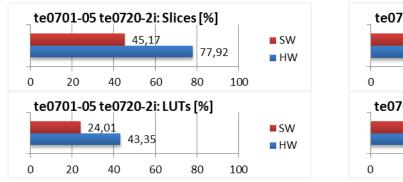


Figure 4: Project sh02 - Edge detection with two HW accelerators

TE0720-02-2IF Sobel 2x

Energy per one frame (SW): 558.58 mJ Energy per one frame (HW): 102.60 mJ Energy per frame reduction: **5.44 x**



10,72 SW 60 HW 0 20 40 60 te0701-05 te0720-2i: BRAMs [%] 20,71 SW 36,43 HW 20 40 60 80 100 te0701-05 te0720-2i: FFs [%] 17,74 SW 33,75 HW 20 40 60 80 100

te0701-05 te0720-2i: FPS

Figure 5: Project sh02 - Energy per frame reduction and used HW resources.



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1.4 Project sh03: Edge detection with three HW accelerators

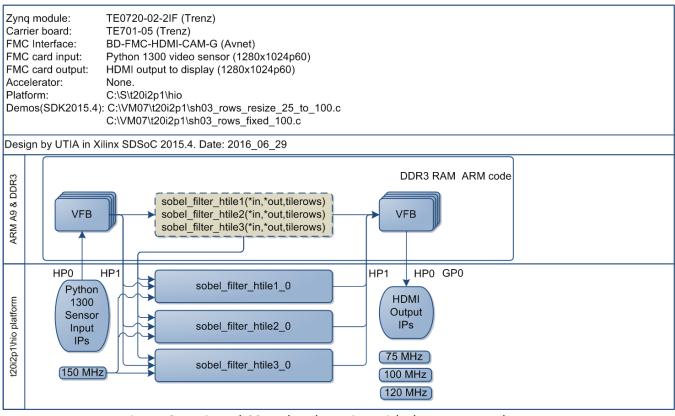
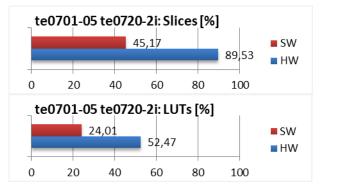
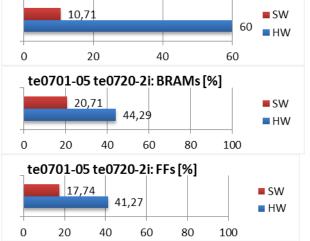


Figure 6: Project sh03 - Edge detection with three HW accelerators

TE0720-02-2IF Sobel 3x

Energy per one frame (SW): 559.1 mJ Energy per one frame (HW): 103.6 mJ Energy per frame reduction: **5.39 x**





te0701-05 te0720-2i: FPS

Figure 7: Project sh03 - Energy per frame reduction and used HW resources.



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1.5 Project md01: Motion detection with single chain of HW accelerators

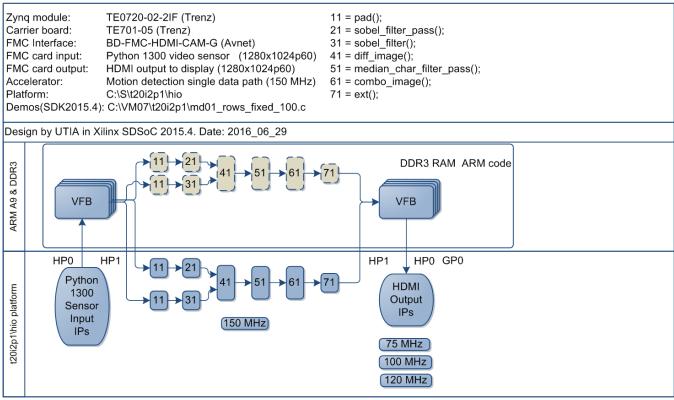


Figure 8: Project md01 - Motion detection with single HW accelerator data path

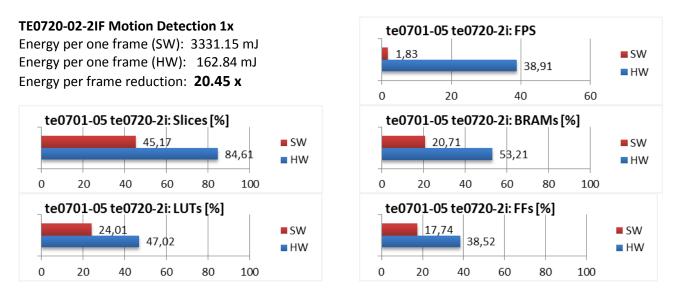


Figure 9: Project so01 - Energy per frame reduction and used HW resources.

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1.6 Project md02: Motion detection with two chains of HW accelerators

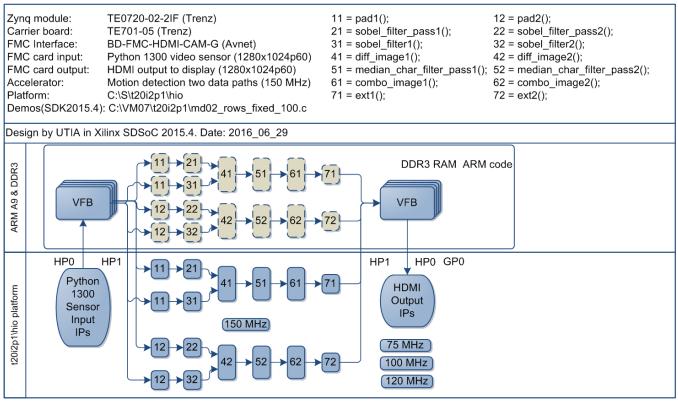


Figure 10: Project md02 - Motion detection with two HW accelerator data paths

TE0720-02-2IF Motion Detection 2x te0701-05 te0720-2i: FPS Energy per one frame (SW): 3331.15 mJ 1,83 SW Energy per one frame (HW): 110.40 mJ 60 HW/ Energy per frame reduction: 30.17 x 0 20 40 60 te0701-05 te0720-2i: Slices [%] te0701-05 te0720-2i: BRAMs [%] 45,17 20,71 SW SW 98,87<mark>_</mark> HW 85,71 HW 0 60 0 100 40 20 40 20 80 100 60 80 te0701-05 te0720-2i: FFs [%] te0701-05 te0720-2i: LUTs [%] 24,01 SW 17,74 SW 69 58,51 HW HW 0 20 40 60 80 100 0 20 40 60 80 100

Figure 11: Project so02 - Energy per frame reduction and used HW resources.



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2. Installation of evaluation package

2.1 Import of SW projects in Xilinx SDK 2015.4

Unzip the evaluation package to directory of your choice. The directory C:\VM_07 will be used in this application note. C:\VM_07\t20i2p1_V54_IMPORT

Create empty directory for Xilinx SDK workspace. C:\VM_07\t20i2p1

Start Xilinx SDK 2015.4 and select the directory for the SDK 2015.4 workspace. See Figure 12. Select C:\VM_07\t20i2p1

Workspace Launcher	
Select a workspace	
Xilinx SDK stores your projects in a folder called a workspace. Choose a workspace folder to use for this session.	
Workspace: C:\VM07\t20i2p1	Browse
Use this as the default and do not ask again	OK Cancel

Figure 12: Select the SDK Workspace

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HW and SW projects can be imported into SDK now. Select:

File -> Import -> General -> Existing Projects into Workspace Click on Next button. See Figure 13.



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SOK Import	
Select Create new projects from an archive file or directory.	Ľ
Select an import source: type filter text	
 ✓ General ☑ Archive File ☑ Existing Projects into Workspace ☑ File System ☑ Preferences ▷ ☑ C/C++ ▷ ☑ Git ▷ ☑ Install ▷ ☑ Remote Systems ▷ ☑ Run/Debug ▷ ☑ Team ▷ ☑ Tracing 	
Sack Next > Finish	Cancel

Figure 13: Import Existing Projects into Workspace

Type directory with projects to be imported. See Figure 14.

C:\VM_07\t20i2p1_V54_IMPORT

Set the "Copy projects into workspace" check box.

Click on Finish button. See Figure 14.

Process of compilation will start automatically. This first compilation of all SDK SW projects can take several minutes to finish. It should finish without errors.

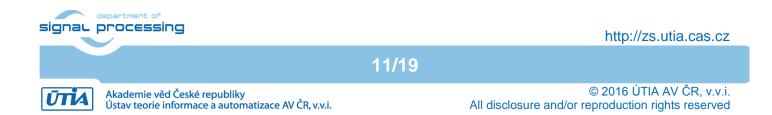
10/19





SOK Import			_ D _ X
Import Projects Select a directory to sear	ch for existing Eclipse projects.		
Select archive file:	C:\VM07\t20i2p1_V54_IMPORT	•	Browse Browse
 md01_bsp (C:\VN md01_hw_platfor md01_rows_fixed md02_bsp (C:\VN md02_hw_platfor md02_rows_fixed sh01_bsp (C:\VM sh01_hw_platforr sh01_rows_fixed_i sh01_rows_resize_i sh02_bsp (C:\VM sh02_hw_platforr sh02_rows_fixed_i sh02_rows_resize_i sh02_rows_resize_i sh03_hw_platforr sh03_rows_fixed_i 	<pre>\\t20i2p1_V54_IMPORT\edkdsp) /07\t20i2p1_V54_IMPORT\md01_bsp) rm_0 (C:\VM07\t20i2p1_V54_IMPORT\md01_nw_platform_0) _100 (C:\VM07\t20i2p1_V54_IMPORT\md01_rows_fixed_100) /07\t20i2p1_V54_IMPORT\md02_bsp) rm_0 (C:\VM07\t20i2p1_V54_IMPORT\md02_nw_platform_0) _100 (C:\VM07\t20i2p1_V54_IMPORT\md02_rows_fixed_100) 07\t20i2p1_V54_IMPORT\sh01_bsp) n_0 (C:\VM07\t20i2p1_V54_IMPORT\sh01_nows_fixed_100) _25_to_100 (C:\VM07\t20i2p1_V54_IMPORT\sh01_rows_fixed_100) _25_to_100 (C:\VM07\t20i2p1_V54_IMPORT\sh01_rows_resize_25_to_100) 07\t20i2p1_V54_IMPORT\sh02_bsp) n_0 (C:\VM07\t20i2p1_V54_IMPORT\sh02_nows_fixed_100) _25_to_100 (C:\VM07\t20i2p1_V54_IMPORT\sh02_rows_fixed_100) _25_to_100 (C:\VM07\t20i2p1_V54_IMPORT\sh02_rows_resize_25_to_100) 07\t20i2p1_V54_IMPORT\sh03_p) n_0 (C:\VM07\t20i2p1_V54_IMPORT\sh03_nows_resize_25_to_100) 07\t20i2p1_V54_IMPORT\sh03_hw_platform_0) 100 (C:\VM07\t20i2p1_V54_IMPORT\sh03_nows_fixed_100) _25_to_100 (C:\VM07\t20i2p1_V54_IMPORT\sh03_rows_resize_25_to_100)</pre>		Select All Deselect All Refresh
Options Search for nested pro Copy projects into w Working sets Add project to work Working sets:	orkspace	•	Select
?	< Back Next > Finish		Cancel

Figure 14: Select "Copy projects into workspace" and finish the import of all projects.



C/C++ - Xilinx SDK	1000	_ D _X
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▷ 25 md01_rows_fixed_100 ▷ 10 md02_bsp		
b ∰ md02_hw_platform_0		
p p md02_rows_fixed_100		
⊳ 🏙 sh01_bsp		
> 5 sh01_rows_resize_100		
b 🏙 sh02_bsp		
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b pm sh02_tows_resize_23_t0_t00 b pm sh03_bsp		
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QEMU TcfGdbClient Control Contro Control Control Control Control Control C		8:57:57 INFO
09:02:32 Build Finished (took 1s.653ms)		
	-	-
<	•	4

Figure 15: All projects are compiled in debug mode.

SDK 2015.4 compiles SW of all imported demos in debug mode.

2.2 HW setup

HW setup is using commercially accessible components [1], [2], [3], [4], [5]:

TE0720-03-2IF; Part: XC7Z020-2CLG484I; 1 GByte DDR; Industrial Grade;	Price: €269,00 [1]
Heatsink for TE0720, spring-loaded embedded;	Price: €19.00 [2]
TE0701-05 Carrier Board for Trenz Electronic 7 Series;	Price: €249.00 [3]
AES-FMC-HDMI-CAM-G FMC card with HDMI I/O and CAM interface	Price: \$250.00 [4]
AES-CAM-ON-P1300C-G PYTHON-1300 color image sensor	Price \$499.00 [5]

HW Options:

signal processing

TE0720-03-2IF	can be replaced by	TE0720-02-2IF
TE0701-05	can be replaced by	TE0701-04

(Same Price, both boards from Trenz) [1]. (Same Price, both boards from Trenz) [3].

Trenz TE0701-04 or TE0701-05 carriers require modifications to run the FMC Imageon carrier AES-FMC-HDMI-CAM-G with Zynq TE0720-03-2IF system on module. The modification is related to the swapped polarity of the differential clock signal for the FMC board. Evaluation HW systems with carriers TE0701-04 or TE0701-05 provided by UTIA have these modifications already done.

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UTIA can implement these HW modifications for the original Trenz TE0701-04 and TE0701-05 carriers. This requires written e-mail request to <u>kadlec@utia.cas.cz</u>. Request will be first confirmed by UTIA. The interested party has to cover the cost of shipment of the carrier board to/from UTIA. Modification can be done in 5 working days and it is offered free of charge.

2.3 Test demos

To test demos follow these steps:

- Insert the PYTHON-1300 color image sensor to the connector on the Imageon board.
- Connect monitor supporting 1280x1024p60 resolution by HDMI cable to the HDMI OUT on the Imageon FMC card.
- Switch the monitor ON.
- Connect the carrier board by USB-to-microUSB cable to PC to support JTAG serial link and the standard serial terminal.
- Connect power supply (DC 12V).
- Open and configure the standard serial terminal client (PuTTY or similar) on PC. (Speed: 115200 baud; Data bits: 8; Stop bits: 1; Parity: None; Flow control: None.)
- Reset the board. Board will start first stage boot loader from internal flash as set up by Trenz. It is writing messages to the serial terminal. On request, "Hit any key to stop autoboot" type any key to stop the auto-boot of linux.
- If you need to switch-off the power, close first the serial terminal on the PC. This will help to avoid problems

B COM3 - PuTTY	- • ×
	A
U-Boot 2013.01-00011-gc260602-dirty (Apr 11 2014 - 06:18:54)	
I2C: ready	
DRAM: 256 MiB	
WARNING: Caches not enabled	
MMC: zynq_sdhci: 0	
Using default environment	
In: serial	
Out: serial	
Err: serial	
Net: Gem.e000b000	
Hit any key to stop autoboot: 0	
zynq-uboot>	

Figure 16: Serial console. Reset board and stop autoboot.

Download bitstream to the board. Demo sh01_rows_fixed_100 will be used as an example. The bitstream.bit for demo sh01 is located in the directory: C:\VM_07\ t20i2p1\sh01_hw_platform_0



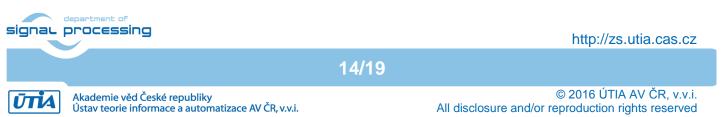
SOK Program FPGA	
Program FPGA Specify the bitstream	n and the ELF files that reside in BRAM memory
Hardware Configura	tion 🛁 🗖
Hardware Platform:	sh01_hw_platform_0
Connection:	Local New
Device:	Auto Detect Select
Bitstream:	C:\VM07\t20i2p1\sh01_hw_platform_0\bitstream.bit Search Browse
Partial Bitstream	
BMM/MMI File:	Search Browse
Software Configurati	ion
Processor	ELF/MEM File to Initialize in Block RAM
?	Program Cancel

Figure 17: Download bitstream to the PL part of Zynq.

Select Program to download the bitstream to the PL part of Zynq via the USB cable in JTAG mode.

Debug Configurations			×
Create, manage, and run configurations			Ť.
Vype filter text Target Communication Framework Xilinx C/C++ application (GDB) Xilinx C/C++ application (System Debugger on QEMU) Xilinx C/C++ application (System Debugger)	Debug Type: Standalo Connection: Local Device: Auto De	Application & Source & STDIO Connection & one Application Debug	
Filter matched 6 of 16 items			Apply Revert
?			Debug

Figure 18: Select demo application for debug.



🔯 Debug - sh01_rows_fixed_100/src/main.c - Xilinx SDK		
File Edit Source Refactor Navigate Search Project Xilinx Tools Run Window Help		
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\$ sh01_rows_fixed_100 Debug [Xilinx C/C++ application (GDB)]		🗄 🐗 🖃 🖋 💥 🙀 📑 😚 💙
XMD Target Debug Agent (05.07.16 9:14) (Suspended)	Name	Value
 Image: Second secon	(×)= status	1680352
arm-xilinx-eabi-gdb (05.07.16 9:14)	(×)= key	0
C:\VM07\t20i2p1\sh01_rows_fixed_100\Debug\sh01_rows_fixed_100.elf (05.07.16 9:14)	(x)= menu_print_en	0
••••••••••••••••••••••••••••••••••••	•	III •
		Ψ.
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le main.c ⊠		🗄 Outline 🛛 📃 🗖
}	•	🖹 hange 🕺 🖉 🔁
<pre>#include "frame size.h"</pre>		🚽 stdio.h 🔺
//#include "image_cores.h"		stdlib.h
		2 xil_cache.n
⊖int main() {		xparameters.h platform.h
int status;		ui.h
u8 key;		img_filters.h
<pre>uo key; uo menu print en = 1;</pre>		# 12C_BASE
		# DDR_MEM_BASE
<pre>init_platform();</pre>	-	🚽 sds_lib.h 🗸
•	Þ	4 III +
📥 Target Conne 🛱 🗖 🗖 📮 Console 🕅 🧟 Tasks 💻 SDK Terminal 튍 Problems	s 🚺 Executables 📋 Memory 👘 🗖	🔄 SDK Log 🛛 📑 📑
	· 🔌 📴 🖬 🖅 🖳 🛨 🔂 🛨	09:11:32 INFO : Connected to
b Hardware Server sh01_rows_fixed_100 Debug [Xilinx C/C++ application (GDB)] C:\VM07\t20i2p1\sh01_rows_fixed_100\Debu		
▷ Continue TCF Agent Process STDIO not connected to console. 09:11:35 INFO : FPGA configure		
> QEMU TcfGdbClient If you'd like to see UART output in this const	ole, please modify STDIO setting	09:14:12 INF0 : ps7_init is c 09:14:12 INF0 : ps7_post_conf
		09:14:12 INFO : Processor res
<	-	4 III +

Figure 19: Debug stops at first executable line of Arm Cortex A9 code.

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- All evaluation demos can be also compiled into Release versions with optimisation set to -O2 or -O3.
- All evaluation demos can boot directly from SD card. FSBL projects can use the standard project template as provided by the SDK 2015.4
- Demo sh01_rows_fixed_100 works on complete frame with single HW accelerator data path
- Demo **sh01_rows_resize_25_to_100** works with identical HW. But SW scales dynamically the number of lines to be processed. This is scaling from ¼ of frame to the complete frame. Part of the frame which is not processed is automatically propagating the input video signal via the cyclic structure of 8 video frame buffers. The HW data movers are instructed about the number of lines to be processed. SW is writing this information to an AXI-lite configuration register of the data mover IP core.
- Demos sh02_rows_fixed_100 and sh02_rows_resize_25_to_100 work with 2 data paths.
- Demos sh03_rows_fixed_100 and sh03_rows_resize_25_to_100 work with 3 data paths.
- Demos md01_rows_fixed_100 and md02_rows_fixed_100 work with one and two HW video processing chains. These HW chains have only fixed set of processed lines (1x 100% and 2x 50% of the frame).

Files for the SD card (SW implementation of video processing algorithms on Arm in SDSoC 2015.4) can be found in:

SD_cards\SW\sh01\BOOT.bin SD_cards\SW\sh02\BOOT.bin SD_cards\SW\sh03\BOOT.bin SD_cards\SW\md01\BOOT.bin SD_cards\SW\md02\BOOT.bin

These files can be used for evaluation of the system performance in case of sequential SW computation on Arm Cortex A9 processor without HW acceleration. Projects have been compiled with maximal optimisation (-O3) without use of NEON.

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3. References

- [1] TE0720-03-2IF; Part: XC7Z020-2CLG484I; 1 GByte DDR; Grade: Industrial; Price: €269,00. <u>http://shop.trenz-electronic.de/en/TE0720-03-2IF-Xilinx-Zynq-module-XC7Z020-2CLG484I-ind.-</u> <u>temp.-range-1-Gbyte</u>
- [2] Heatsink for TE0720, spring-loaded embedded; Price: €19.00. https://shop.trenz-electronic.de/en/26922-Heatsink-for-TE0720-spring-loaded-embedded?c=38
- [3] TE0701-05 Carrier Board for Trenz Electronic 7 Series; Price: €249.00. <u>https://shop.trenz-electronic.de/en/TE0701-05-Carrier-Board-for-Trenz-Electronic-7-Series</u>

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- [4] AES-FMC-HDMI-CAM-G Price: \$250.00. http://products.avnet.com/shop/en/ema/3074457345623664802
- [5] AES-CAM-ON-P1300C-G •PYTHON-1300 color image sensor Price \$499.00 https://products.avnet.com/shop/en/ema/development-kits/3074457345623664700



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4. Evaluation license

The **evaluation version of the package** can be downloaded from UTIA www pages free of charge for evaluation of HW accelerated edge detection and motion detection algorithms for the Python 1300 video sensor on TE0720-03-2IF module [1] located on TE0701-05 carrier [3].

The evaluation package includes SDK 2015.4 SW projects with C source code for Arm Cortex A9 processor (32bit) in standalone mode.

The evaluation package includes these static libraries for Arm Cortex A9 processor (32bit) for standalone mode:

libfmc_imageon.a	SDK 2015.4 UTIA static library with interface functions for video IP cores
libsh01.a	SDSoC 2015.4 static library for HW accelerator in project sh01
libsh02.a	SDSoC 2015.4 static library for HW accelerator in project sh02
libsh03.a	SDSoC 2015.4 static library for HW accelerator in project sh03
libmd01.a	SDSoC 2015.4 static library for HW accelerator in project md01
libmd02.a	SDSoC 2015.4 static library for HW accelerator in project md02

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These libraries have no time restriction.

Source code of these libraries is not provided in this evaluation package.



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