Application Note

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Floating Point Accelerators for MicroBlaze - Partial Runtime Reconfiguration

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Contents

Revision history

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0	9.12.2008	Lukáš Kohout	Document creation
1			
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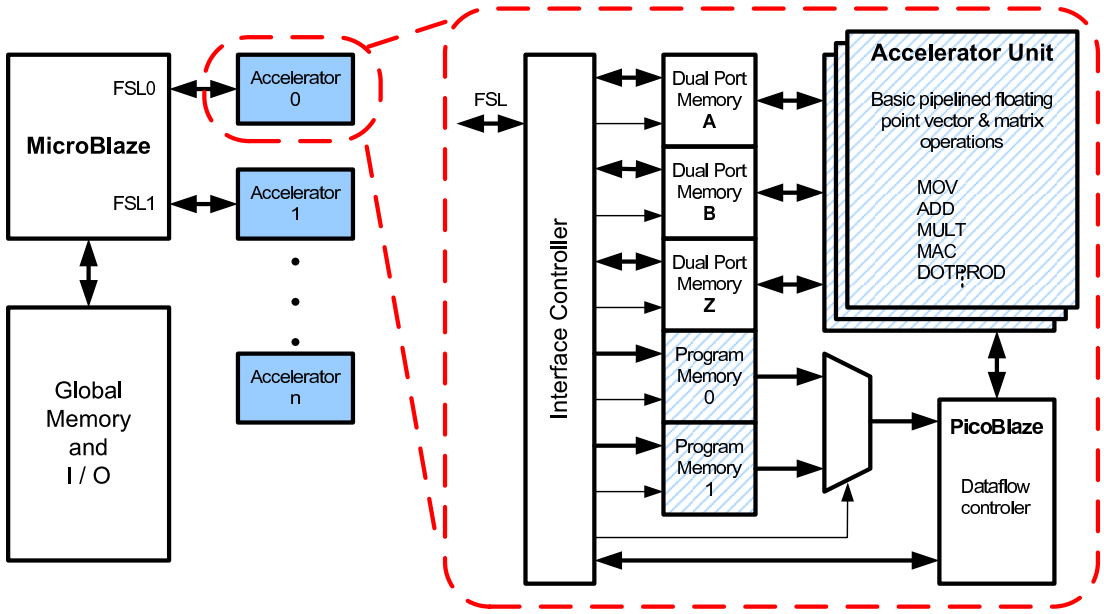

Figure 1: Block diagram of the UTIA HW Platform

1 Introduction

Due to the advance of technology at present we can perceive partial runtime reconfiguration of FPGAs as another architectural feature ready to be used in real-world designs, both the FPGA silicon and design tools are available today. The text describes an reconfigurable extension of a generally reprogrammable platform (UTIA HW Platform [1]).

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2 Description

An application is based on the UTIA HW platform [1], configurable platform based on the Xilinx EDK and Xilinx System Generator tools. The platform is built around a MicroBlaze processor [4] with a set of standard peripherals such as DDR RAM controller and RS232 interface. This text includes a basic description of the used hardware platform however it is mainly focused on the partial runtime reconfiguration extension.

2.1 UTIA HW Platform

The UTIA HW platform is a heterogenous system based on the MicroBlaze processor [4] with one or more accelerator, the number of the accelerators is limited by FSL (Fast Simplex Link) pairs count or FPGA resources limits. Accelerators support single data path or more SIMD (two, four or eight) identical data paths controlled by a single tiny controller (PicoBlaze processor [5]). The block diagram of the UTIA HW platform is shown in the figure 1. Another information about UTIA HW platform can be found in the [1], [2] or [3].

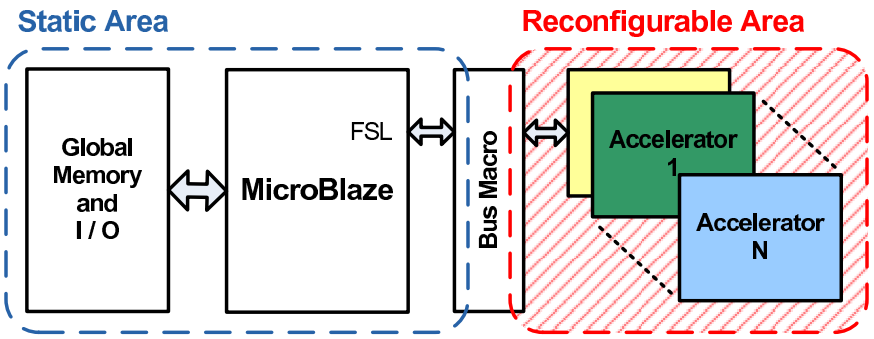

Figure 2: Block diagram of the UTIA HW Platform with one reconfigurable area.

2.2 Partial Runtime Reconfiguration

In a partial-runtime-reconfiguration designs is an implemented system split on two areas, static and reconfigurable areas. In the static area is a basic system with configuration controller, the reconfigurable area provides time sharing of the FPGA resources, design parts which are placed in can be swapped on the fly. Both the static and the reconfigurable areas are separated with a bus macro. It is possible to has more than one reconfigurable area in the design. The block diagram of the reconfigurable platform is shown in the figure 2.

3 Implementation

The application is implemented with ML402 Evaluation Platform [6] (Xilinx Virtex-4 SX35). Base system (static area) contains MicroBlaze CPU 6.00.b, FPU, 64 MB DDR SDRAM, Xilinx UART Lite 115.2 Kbps, Central DMA block, HW ICAP (Internal Configuration Access Port) and System ACE. The system clock is 100 MHz. The system contains one reconfigurable area where can alternate two types of the accelerator:

1. single precision floating point SIMD accelerator (2x ADD, 2x MUL),
2. double precision floating point accelerator (1x ADD, 1x MUL).

3.1 Used Tools and Resources

The application was compiled with Xilinx tools, ISE 9.1.03i, ISE 9.1.02i_PR2 and EDK 9.1.02i. Used resources are shown in the table 1, Xilinx FPGA Editor screen with routed design for Xilinx Virtex-4 SX35 is shown in the figure 3.

Used FPGA Resources	FFs	LUTs	DSP48s	RAMB16s	SLICEs
Total on XC4VSX35-10	30 720	30 720	192	192	15 360
Total in reconfigurable area	9 728	9 728	64	64	4 864
Base system, FP in HW	3 854	5 530	7	39	3 247
Single precision SIMD floating point					
fp01_1x2_mac_dot_dot2	2 285	5 335	8	14	3 891
Double precision floating point					
dp01_1x1_mac_dot	3 102	5 771	16	14	4 491

Table 1: Used resources of the Virtex-4 SX35

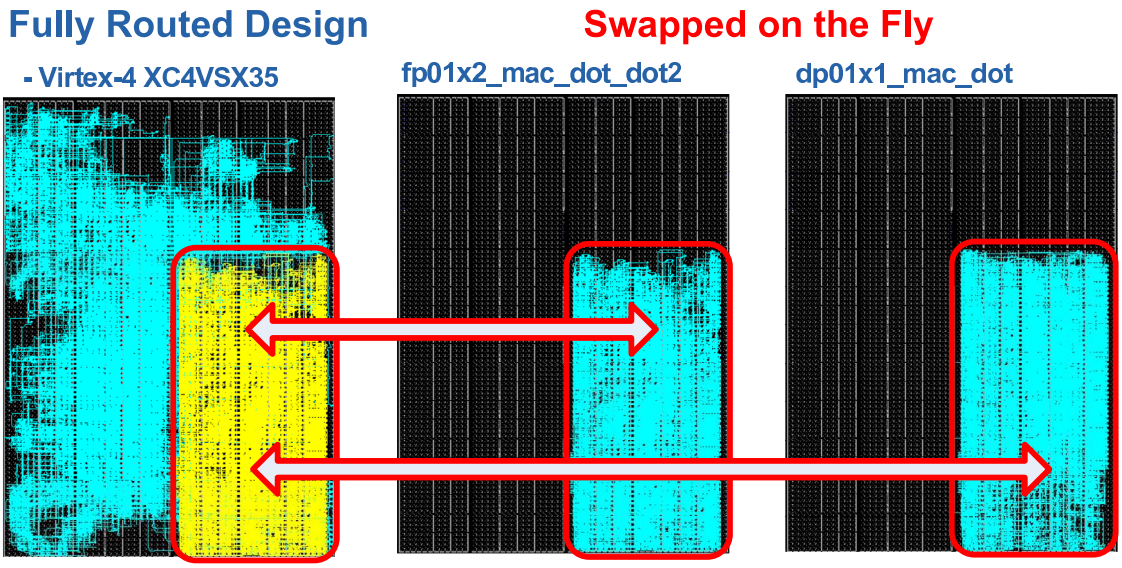

Figure 3: Xilinx FPGA Editor screen for Xilinx Virtex-4 SX35.

3.2 Application Results

During the application starting (see the chapter 4) the partial bitstreams are loaded from compact flash into to the DDR SDRAM. After inicializing the user menu is printed in the software terminal, the user has four pissible options (figure 4):

1. place single precision SIMD floating point accelerator into the reconfigurable area,
2. place double precision floating point accelerator into the reconfigurable area,
3. start computing,
4. exit the program.

If chosen accelerator is not placed in the reconfigurable area yet, the partial runtime reconfiguration is done. At opposite case is nothing happened. During every partial runtime reconfiguration the reconfiguration latency is measured. The results are in the table 2. The table 2 also includes a pure PicoBlaze reprogramming latency for the comparing with the partial runtime reconfiguration latency.

	Partial bitstream size [B]	**Reconfiguration latency [us]**	**Load PB program latency (4096 B) [us]**
Single precision SIMD floating point			
fp01_1x2_mac_dot_dot2	358 520	88 906	93
Double precision floating point			
dp01_1x1_mac_dot	357 240	88 590	93

Table 2: Reconfiguration and reprogrammation latencies.

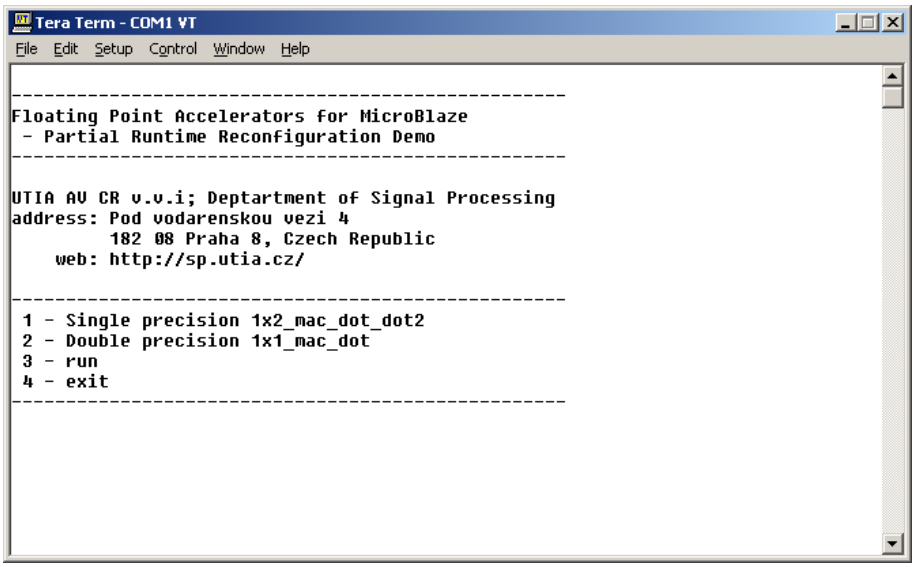

Figure 4: The application user menu.

4 Application Start

A bundled CD contains a programing file for System ACE and partial bitfiles in folder `CF_files/`, see the chapter 5).

Application results are reported by a software terminal, same as in standard MicroBlaze systems. Software terminal settings are in the table 3.

Steps necessery for appliction running are in the next list:

1. Copy files from `CF_files/` folder into a compact flash card (CF card).
2. Plug in the CF card to a ML402 board.
3. Connect the ML402 board with RS232 link in your PC (5).
4. Set the software terminal according to the table 3.
5. Switch on power on the ML402 board.
6. Push the reset button on the ML402 bord because of known reset issue by System ACE using (5).
7. Observe the software terminal.

Baud rate	115200
Data	8 bit
Parity	none
Stop bit	1 bit
Flow control	none

Table 3: Software terminal settings

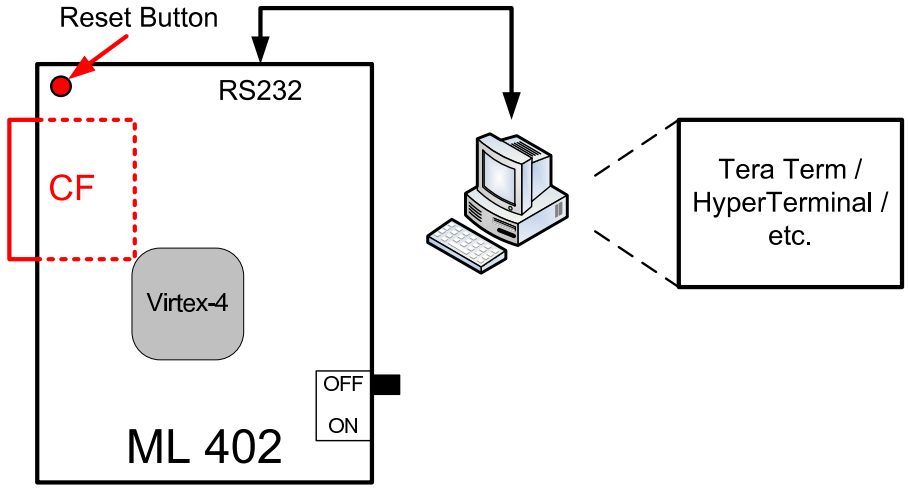

Figure 5: ML-402 connection

5 Package Contents

```
.
|-- CF_files/
|    |-- reconf.ace
|    |-- rmod_0.bit
|    `-- rmod_1.bit
|-- doc/
`-- readme.txt
```

References

[1] Kadlec, Jiří ; Bartosinski, Roman ; Daněk, Martin. *Accelerating MicroBlaze Floating Point Operations*. In Proceedings 2007 International Conference on Field Programmable Logic and Applications (FPL). Delft : IEEE, 2007. S. 621-624. ISBN 1-4244-1060-6. [International Conference on Field Programmable Logic and Applications. FPL 2007, Amsterdam, 27.08.2007-29.08.2007, NL].

[2] Daněk, Martin ; Kadlec, Jiří ; Bartosinski, Roman ; Kohout, Lukáš. *Increasing the Level of Abstraction in FPGA-based Designes*. In International Conference on Field Programmable Logic and Applications. Heidelberg : Kirchhoff Institute for Physics, 2008. S. 5-10. ISBN 978-1-4244-1961-6. [International Conference on Field Programmable Logic and Applications, Heidelberg, 08.09.2008-10.09.2008, DE]. `http://library.utia.cas.cz/separaty/2008/ZS/danek-increasing%20the%20level%20of%20abstraction%20in%20fpga-based%20designes.pdf`.

[3] Kadlec, Jiří ; Daněk, Martin ; Kohout, Lukáš. *Proposed architecture of configurable, adaptable SoC*. In The IET Irish Signals and Systems Conference ISSC 2008. Londýn : Institution of Engineering and Technology, 2008. S. 368-373. ISBN 978-0-86341-931-7. [The Institution of Engineering and Technology Irish Signals and Systems Conference, ISSC 2008, Galway, 18.06.2008-19.06.2008, IE]. `http://library.utia.cas.cz/separaty/2008/ZS/kohout-architectures%20of%20digital%20self-adaptive%20systems.pdf`.

[4] Xilinx. *MicroBlaze Processor Reference Guide, Embedded Development Kit EDK 9.1i, v7.0*. `http://www.xilinx.com` [online] `http://www.xilinx.com/support/documentation/sw_manuals/edk91i_mb_ref_guide.pdf`, September 15, 2006.

[5] Xilinx. *PicoBlaze 8-bit Embedded Microcontroller User Guide for Spartan-3, Virtex-II, and Virtex-II Pro FPGAs, UG129 (v1.1.1)*. `www.xilinx.com` [online] `http://www.xilinx.com/bvdocs/userguides/ug129.pdf`, November 21, 2005.

[6] Xilinx. *ML401/ML402/ML403 Evaluation Platform, User Guide, v2.5*. `www.xilinx.com` [online] `http://www.xilinx.com/support/documentation/boards_and_kits/ug080.pdf`, May 24, 2006.