Application Note

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Evaluation of FP27 SIMD Lattice HW IP on ZCU104 board

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Revision history

Rev.	Date	Author	Description
V1.0	31/05/2026	J. Kadlec	Evaluation release for SOIL project

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PROJECT INFORMATION

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1 Introduction

In Chip JU project SOIL, in WP3, UTIA develops SIMD HW IP for acceleration of adaptive RLS Lattice filter with recursively estimated 1024 coefficients. It will be used in WP5 UTIA demonstrator for the adaptive acoustic noise cancellation.

This application note describes use of evaluaton package released by UTIA 31.5.2026. The performance of the RLS Lattice can be evaluated on ZCU104 board.

- The evaluation design has been created in latest AMD Vitis 2025.2 tool chain. It demonstrates:
  - Performance of the RLS Lattice filter app accelerated by FP27 SIMD HW IP.
  - Performance of the RLS Lattice filter app running on single core of A53 PS.
  - Performance of the RLS Lattice filter app running on four cores of A53 PS.
- These 3 Apps can be modified by the user, recompiled in Vitis 2025.2 GUI and tested on the ZCU104 board.
- The RLS Lattice firmware for the FP27 SIMD HW IP can be modified by the user, recompiled in Vitis 2025.2 GUI and tested on the ZCU104 board.
- The A53 PS (1.2 GHz) is running Linux. The RLS Lattice HW IP (300 MHz) is instantiated in the PL part of the device.
- The evaluation package is using as reference the RLS Lattice coefficient estimation sequence and forward and backward prediction error signals computed in Matlab offline from off line measured **12.276 s of acoustic data sampled at 32 kHz**. Matlab computation of RLS Lattice has been performed off line with FP27 arithmetic (ADD, SUB, MUL and DIV).
- This off line computed RLS Lattice coefficient estimation sequence and the forward and backward prediction error signals are used verify correctness of:
  - Computation of the RLS Lattice filter app accelerated by FP27 SIMD HW IP.
  - Computation of the RLS Lattice filter app running on single core of A53 PS.
  - Computat ion of the RLS Lattice filter app running on four cores of A53 PS.
- The app computing time is:
  - RLS Lattice filter app accelerated by FP27 SIMD HW IP 8.567 s.
  - RLS Lattice filter app running on single core of A53 PS 139.810 s.
  - RLS Lattice filter app running on four cores of A53 PS 49.279 s.
- The acceleration by by FP27 SIMD HW IP is:
  - RLS Lattice filter app accelerated by FP27 SIMD HW IP 1.000 x reference.
  - RLS Lattice filter app running on single core of A53 PS **15.319 x slower**.
  - RLS Lattice filter app running on four cores of A53 PS **4.752 x slower.**
- The demonstrated system running on the ZCU104 board with the RLS Lattice filter app. accelerated by the FP27 SIMD HW IP can perform the active noice cancellation in the real time (as 8.567 s < 12.276 s) for the adaptive RLS Lattice filter with 1024 coefficients and the data sampling rate 32 kHz.

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2 Reproduction of reported performance results

2.1 Create evaluation SD card

This application note is accompanied with the evaluation package

22_04_Vitis_2025_2_PL_AI_6_1_zcu104_2x_v2_SD.zip (size 2 749 039 782 bytes).

Please, dowload the evaluation package from UTIA www server dedicated to SOIL project:

https://zs.utia.cas.cz/index.php?ids=projects/soil

unzip the package to a directory

22_04_Vitis_2025_2_PL_AI_6_1_zcu104_2x_v2_SD

The content of the package is described, now.

The sdk.sh is the sysroot archive needed by Vitis 2025.2 for crosscompilation

```
Directory .\22_04_Vitis_2025_2_PL_AI_6_1_zcu104_2x_v2_SD
25/04/2026  11:17     1,756,217,040 sdk.sh
```

The three files with file name started with 388d… are the precompiled A53 PS apps.
The archive.zip is an Vitis 2025.2 project archive with source code of these three apps.
The sd_card.zip is compressed SD card image, needed to boot the ZCU104 board.
It contains the integrated evaluation version of the FP27 RLS Lattice HW IP in the PL part of the device.

```
Directory .\ZCU104_04d_388d_2x_fp23d4f2u_1f_v2_xrt_300_sw
30/05/2026  18:38        17,965,656 388d_2x_fp23d4f2u1d_1f_hw1_host
30/05/2026  18:41        17,989,352 388d_2x_fp23d4f2u1d_1f_sw1_host
30/05/2026  18:44        17,989,376 388d_2x_fp23d4f2u1d_1f_sw4_host
15/05/2026  10:41        79,319,812 archive.zip
29/05/2026  14:47       901,857,484 sd_card.zip
```

These files are needed by the Vitis platform for the initial boot of the A53 PS.

```
Directory .\ZCU104_SDK\pfm\boot
25/04/2026  08:33            99,272 bl31.elf
25/04/2026  08:47           749,008 fsbl.elf
25/04/2026  08:49           901,264 pmufw.elf
25/04/2026  08:32            74,103 system.dtb
25/04/2026  08:37         1,561,752 u-boot.elf
```

These files are needed for the system boot.

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```
Directory .\ZCU104_SDK\pfm\sd_dir
25/04/2026  08:33             3,833 boot.scr
25/04/2026  08:32            74,103 system.dtb
```

Unzip the sd_card.zip archive to the **`sd_card.img`** (5,319,426,048 Bytes).

```
Directory .\ZCU104_04d_388d_2x_fp23d4f2u_1f_v2_xrt_300_sw
30/05/2026  18:38        17,965,656 388d_2x_fp23d4f2u1d_1f_hw1_host
30/05/2026  18:41        17,989,352 388d_2x_fp23d4f2u1d_1f_sw1_host
30/05/2026  18:44        17,989,376 388d_2x_fp23d4f2u1d_1f_sw4_host
15/05/2026  10:41        79,319,812 archive.zip
29/05/2026  14:36     5,319,426,048 sd_card.img
29/05/2026  14:47       901,857,484 sd_card.zip
```

2.2 Write the SD card

Write **`sd_card.img`** to the SD card using SD card reader.

In Windows 11 Pro PC, install program **`Win32DiskImager`** for this task.
Win32 Disk Imager can write raw disk image to removable devices.
https://win32diskimager.org/

2.3 Test HW accelerated FP27 RLS Lattice app

Connect the Display Port monitor, keyboard and mouse to the ZU104 board.

Insert SD card to the ZCU104 board.

Swith the board ON.

Menu is open on the Display Port monitor.

Select by mouse the Rxvt Terminal icon

In the rxvt terminal, change the directory and run the test app:

```
cd /run/media/mmcblk0p1/

./388d_2x_fp23d4f2u1d_1f_v2_xrt_300_host -x binary_container_1.xclbin

Open the device0
Load the xclbin binary_container_1.xclbin
Program steps = 5474
Copying data...
Launching Kernel...
Getting Results...
Prepare ...
2 DPUs, Lattice filters: 1x256 threads, float. 1000 blocks. ...
TEST of B1_B8 PASSED
```


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```
Lattice ...
Finish ...
TEST of Lattice filter 1 var 1: PASSED
TEST of Lattice filter 1 var 2: PASSED
TEST of Lattice filter 1 var 3: PASSED
TEST of Lattice filter 1 var 4: PASSED
Compute Lattice in 256 threads:
elapsed_prepare          =            21.020908
elapsed_lattice          =            8.622026
elapsed_finish           =            0.446375
License and properties:
properties1              =            c013ff00
properties2              =            c013ff00


root@xilinx-zcu104-20252:/run/media/mmcblk0p1#
```

The RLS Lattice has been computed in 8.622 s and verification tests have PASSED.

Close the terminal by mouse or by typing:

```
exit
```

Cloase the file system and halt processor by clicking on the icon Shutdown .

Swith power off and remove the SD card.

2.4 Test SW versions of the FP27 RLS Lattice app

In PC, select fixed Etherneet address to 192.168.0.2 .

Connect ZCU104 with PC by Ethernet cable.

Insert SD card to the ZCU104 board.

Swith the board ON.

Menu is open on the Display Port monitor. Select by mouse the Rxvt Terminal icon.

In Rxvt terminal, configure the ethernet address of the ZCU104 to 192.168.0.10 :

```
ifconfig end0 192.168.0.10
```

In PC, use the utility WinSCP for secure copy from PC to the board via local Ethernet. If needed, download it from https://winscp.net/eng/download.php .

Copy

388d_2x_fp23d4f2u1d_1f_hw1_host
388d_2x_fp23d4f2u1d_1f_sw1_host

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388d_2x_fp23d4f2u1d_1f_sw4_host

to the ZCU104 directory:

/run/media/mmcblk0p1/388d_2x_fp23d4f2u1d_1f_hw1_host
/run/media/mmcblk0p1/388d_2x_fp23d4f2u1d_1f_sw1_host
/run/media/mmcblk0p1/388d_2x_fp23d4f2u1d_1f_sw4_host

The WinSCP utility will require to enter login as

User: root
Pswd: root

In Rxvt terminal, change the directory and list files:

```
cd /run/media/mmcblk0p1/
ls -lr
total 141535
-rwxrwx--- 1 root disk    74103 Jan  1  2015 system.dtb
-rwxrwx--- 1 root disk     3833 Jan  1  2015 boot.scr
-rwxrwx--- 1 root disk 19372240 Jan  1  2015 binary_container_1.xclbin
-rwxrwx--- 1 root disk 32371200 Jan  1  2015 Image
-rwxrwx--- 1 root disk 21197720 Jan  1  2015 BOOT.BIN
-rwxrwx--- 1 root disk 17965680 Jan  1  2015 388d_2x_fp23d4f2u1d_1f_v2_xrt_300_host
-rwxrwx--- 1 root disk 17989376 May 30 16:44 388d_2x_fp23d4f2u1d_1f_sw4_host
-rwxrwx--- 1 root disk 17989352 May 30 16:41 388d_2x_fp23d4f2u1d_1f_sw1_host
-rwxrwx--- 1 root disk 17965656 May 30 16:38 388d_2x_fp23d4f2u1d_1f_hw1_host
root@xilinx-zcu104-20252:/run/media/mmcblk0p1#
```

In Rxvt terminal test the first SW version of RLS Lattice app running on single A53 core:

```
./388d_2x_fp23d4f2u1d_1f_sw1_host -x binary_container_1.xclbin
Open the device0
Load the xclbin binary_container_1.xclbin
Program steps = 5474
Copying data...
Launching Kernel...
Getting Results...
Prepare ...
2 DPUs, Lattice filters: 1x256 threads, float. 1000 blocks. ...
TEST of B1_B8 PASSED
Lattice ...
Finish ...
TEST of Lattice filter 1 var 1: PASSED
TEST of Lattice filter 1 var 2: PASSED
TEST of Lattice filter 1 var 3: PASSED
TEST of Lattice filter 1 var 4: PASSED
Compute Lattice in 256 threads:
```


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```
elapsed_prepare          =          21.101780
elapsed_lattice          =         140.649145
elapsed_finish           =           0.443796
License and properties:
properties1              =         c013ff00
properties2              =         c013ff00
root@xilinx-zcu104-20252:/run/media/mmcblk0p1#
```

The RLS Lattice has been computed in 140.649 s and all verification tests have PASSED.

In Rxvt terminal test the second SW version of RLS Lattice app running on four A53 cores:

```
./388d_2x_fp23d4f2u1d_1f_sw4_host -x binary_container_1.xclbin
Open the device0
Load the xclbin binary_container_1.xclbin
Program steps = 5474
Copying data...
Launching Kernel...
Getting Results...
Prepare ...
2 DPUs, Lattice filters: 1x256 threads, float. 1000 blocks. ...
TEST of B1_B8 PASSEDLattice ...
Finish ..
TEST of Lattice filter 1 var 1: PASSED
TEST of Lattice filter 1 var 2: PASSED
TEST of Lattice filter 1 var 3: PASSED
TEST of Lattice filter 1 var 4: PASSED
Compute Lattice in 256 threads:
elapsed_prepare          =          21.097939
elapsed_lattice          =          50.676947
elapsed_finish           =           0.444961
License and properties:
properties1              =         c013ff00
properties2              =         c013ff00
root@xilinx-zcu104-20252:/run/media/mmcblk0p1#
```

The RLS Lattice has been computed in 50.676 s and all verification tests have PASSED.

The acceleration by HW IP has been demonstrated.

2.5 User change of FP27 RLS Lattice apps in Vitis 2025.2

The FP27 RLS Lattice applications can be modified and recompiled by the user of this evaluation package.

AMD Vitis 2025.2 tool installation is needed on a PC with Ubuntu 22.04 operating system.

The Vitis 2025.2 tool will be cross-compiling against several board/project specific files.

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In Ubuntu 22.04, create the directory:

~/Work/ZCU104_SDK

Copy the directory:

ZCU104_SDK

to the Ubuntu 22.04 directory

~/Work/ZCU104_SDK

Copy the sysroot creation archive

sdk.sh

to the Ubuntu 22.04 directory

~/Work/sdk.sh

In Ubuntu 22.04, open the terminal set the Vitis 2025.2 settings.sh and install the sysroot by:

```
cd ~/Work
source /tools/Xilinx/2025.2/Vitis/settings.sh
./sdk.sh -d /home/devel/Work/ ZCU104_SDK
```

The sysroot is created in the directory:

/home/devel/Work/ ZCU104_SDK/sysroot

In Ubuntu 22.04 create the directory:

~/Work/ ZCU104_04d_388d_2x_fp23d4f2u_1f_v2_xrt_300_sw

Copy the Vitis 2025.2

archive.zip

to the Ubuntu 22.04 directory:

~/Work/ ZCU104_04d_388d_2x_fp23d4f2u_1f_v2_xrt_300_sw/archive.zip

In Ubuntu 22.04, open the terminal set the Vitis 2025l2 settings.sh and start Vitis 2025.2

```
cd ~/Work/ ZCU104_04d_388d_2x_fp23d4f2u_1f_v2_xrt_300_sw
source /tools/Xilinx/2025.2/Vitis/settings.sh
vitis -w . &
```


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Vitis 2025.2. GUI is opened.

Import archive:

~/Work/ ZCU104_04d_388d_2x_fp23d4f2u_1f_v2_xrt_300_sw/archive.zip

The predefined SWprojects are opened.

SW source code can be modified by the user.

Compile platform for hw.

Compile predefined projects to hw.

Copy re-compiled executables from Ubuntu:

388d_2x_fp23d4f2u1d_1f_hw1_host
388d_2x_fp23d4f2u1d_1f_sw1_host
388d_2x_fp23d4f2u1d_1f_sw4_host

To the Win 11 PC.

In Win 11 PC, use the utility WinSCP for secure copy of these precompiled application executables:

388d_2x_fp23d4f2u1d_1f_hw1_host
388d_2x_fp23d4f2u1d_1f_sw1_host
388d_2x_fp23d4f2u1d_1f_sw4_host

to the ZCU104 directory:

/run/media/mmcblk0p1/388d_2x_fp23d4f2u1d_1f_hw1_host
/run/media/mmcblk0p1/388d_2x_fp23d4f2u1d_1f_sw1_host
/run/media/mmcblk0p1/388d_2x_fp23d4f2u1d_1f_sw4_host

The WinSCP utility will require to enter login as

User: root
Pswd: root

Test the recompiled SW applications on ZCU104 as described before.

3 Conclusions

This application note described use of the evaluation package

22_04_Vitis_2025_2_PL_AI_6_1_zcu104_2x_v2_SD.zip

which can be dowload from UTIA www server dedicated to SOIL project:

https://zs.utia.cas.cz/index.php?ids=projects/soil

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This package is provided for evaluation purpose, for free of charge, for public access.
The package contains the evaluation version if the FP27 RLS Lattice HW IP, integrated in the PL part of the ZU07 device on the ZCU104 evaluation board. It has been designed in Vitis 2025.2 tool chain.

In case of your interest in the FP27 RLS Lattice HW IP, please contact

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4 References

Evaluation package 22_04_Vitis_2025_2_PL_AI_6_1_zcu104_2x_v2_SD.zip can be dowload from UTIA www server dedicated to SOIL project:

https://zs.utia.cas.cz/index.php?ids=projects/soil

The ZCU104 board:

https://cz.farnell.com/xilinx/ek-u1-zcu104-g/eval-board-cortex-a53-cortex-r5/dp/3225208

https://www.farnell.com/datasheets/2937626.pdf?_gl=1*12ql8su*_gcl_au*MTYxMTEwMTUyNS4xNzc1NDcyMjIw

https://cz.farnell.com/xilinx/ek-u1-zcu104-g/eval-board-cortex-a53-cortex-r5/dp/3225208#anchorTechnicalDOCS

https://www.farnell.com/datasheets/2842035.pdf?_gl=1*10jtbj8*_gcl_au*MTYxMTEwMTUyNS4xNzc1NDcyMjIw

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