Application Note

ÚTIA Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

Video Input/Output IP Cores for Xilinx ZCU102 with Avnet HDMI Input/Output FMC Module

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Revision history

Rev.	Date	Author	Description
0	04.16.2019	L. Kohout	Initial version of the document
1			
2			

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Acknowledgement

This work has been partially supported from project FitOptiVis, project number ECSEL 783162 and the corresponding Czech NFA (MSMT) institutional support project 8A18013.

1 Introduction

This application note describes video IP cores interfacing a video input and output of the Xilinx ZCU102 evaluation board [1] with Avnet HDMI Input/Output FMC module [2]. The system is designed with Xilinx Vivado 2018.3 tool.

2 Description

This document describes video chain implemented in the Xilinx Zynq UltraScale+ device. The video chain passes a video signal from the HDMI input through the frame buffer to the HDMI output. Both, HDMI input and output are provided by the Avnet HDMI Input/Output FMC module [2]. This video chain is supposed to be used for processing incoming video frames inside the FPGA and display the resultant video on the monitor. Figure 1 shows the top view of the system block design within the Xilinx Vivado 2018.3 tool.

The video chain reads an input video signal from the HDMI input, stores the data from the video signal in the triple frame buffer and reads the data back to display them via HDMI output. It consists of 3 hierarchical blocks - HDMI Input, Video DMA Input/Output and HDMI Output. The input part of the chain can accept the video signal almost with every resolution, the upper limit is 1920x1080p60. The resolution of the output side of the chain is fully configurable up to 1920x1080p60.

2.1 HDMI Input

The HDMI input (*hdmi_in* block in Figure 1) converts an external video signal from the input HDMI codec on the Avnet HDMI FMC module to the AXI stream to pass the video data to the video DMA block. It includes two IP cores, see Figure 2.

- ***im_hdmi_in_0*** IP core reads the video signal in YCrCb 4:2:2 format. This signal includes embedded synchronization pulses. The core unpacks the syncs and provides complete video signal to its output. The core is developed by UTIA.
- ***v_vid_in_axis_0*** IP core converts complete video signal to the AXI stream. The stream is supplemented with signal *tuser*, which represents *start of frame*, and with signal *tlast*. The meaning of this signal is *end of line*. Optionally, this core provides a timing of the input video signal. This core is a standard part of the Vivado 2018.3 tool.

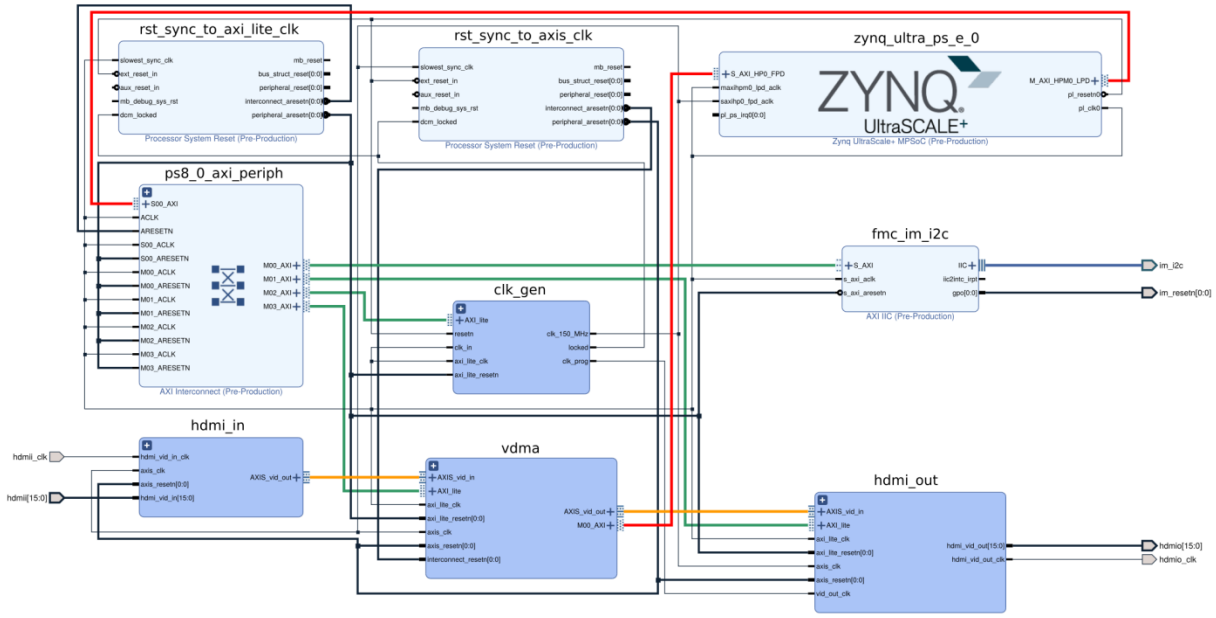


Figure 1: Block design of the whole system in Xilinx Vivado 2018.3 tool.

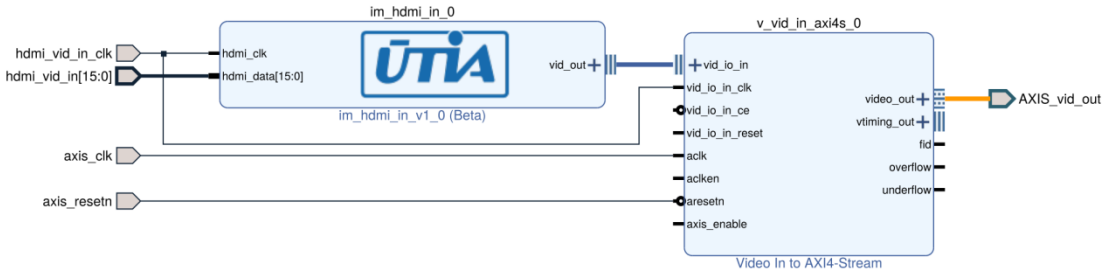


Figure 2: Video Chain - HDMI Input.

2.2 Video DMA Input/Output

The Video DMA (*vdma* block in Figure 1) performs writing of the data from the input AXI stream to the main memory, and reading the data from the memory to feed the output AXI stream, the block includes two IP cores (see Figure 3).

- ***axi_vdma_0*** IP core is configured to have two independent DMAs. The first DMA reads the input AXI stream and writes its data do the frame buffer located in the main memory. The second DMA reads the data from the frame buffer in the main memory and pushes the data to the output AXI stream. This block is configured to store 3 independent frames. It also provides an automatic internal lock among the frames to avoid image tearing. The core can be switched to the manual lock mode in SW application (parking mode) to process the locked frame and returns the resultant frame back to the frame buffer. This core is a part of the Vivado 2018.3 tool.
- ***axi_interconnect_0*** core provides an interconnect between two AXI ports of the *axi_vdma_0* and one AXI high performance port of the Zynq UltraScale+ (its memory controller). This core is a part of the Vivado 2018.3 tool.

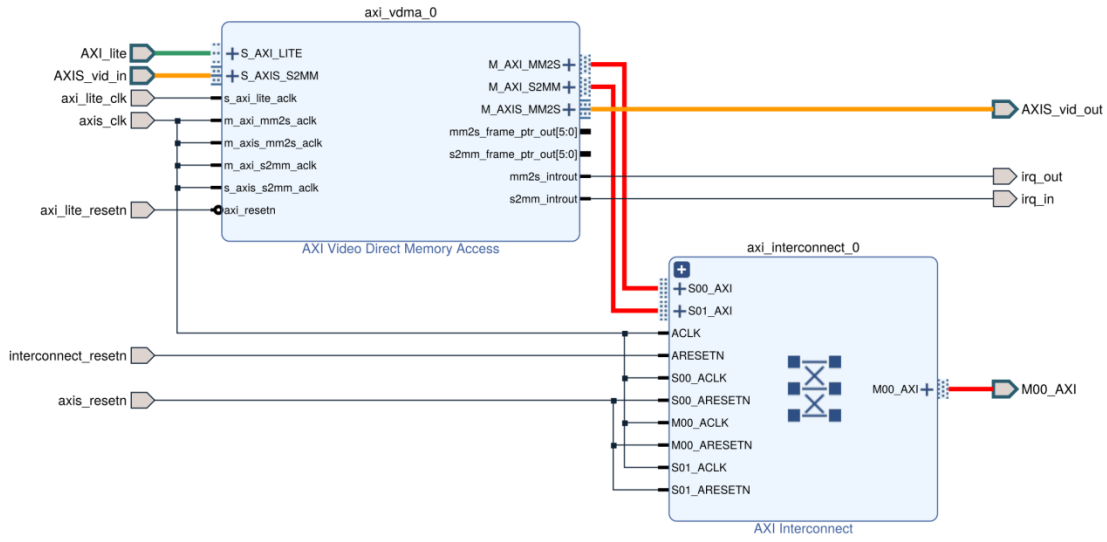


Figure 3: Video Chain - Video DMA.

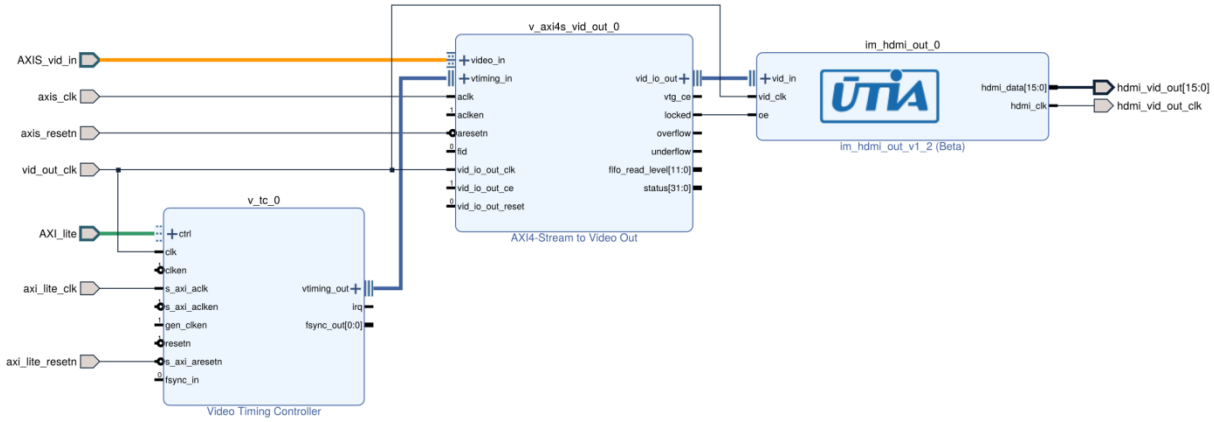


Figure 4: Video Chain - HDMI Output.

2.3 HDMI Output

The HDMI output (*hdmi_out* block in Figure 1) converts an AXI stream from the video DMA block to the video signal which is processed by the output HDMI codec on the Avnet HDMI FMC module. The data of the video signal are coded in YCrCb 4:2:2 format. It is performed by 3 IP cores within the block, they are shown in Figure 4.

- ***v_tc_0*** IP core is a timing controller. It generates synchronization pulses according to required output video resolution and frame rate. This core is a standard part of the Vivado 2018.3.
- ***v_axis_vid_out_0*** IP core gets a video data from the video DMA block via AXI stream and synchronization pulses from the timing controller. It converts the data from the AXI stream to the complete video signal with respect to the required timing. This core is also available in the Vivado 2018.3.
- ***im_hdmi_out_0*** IP core converts a complete video signal with standalone synchronization pulses from the *v_axis_vid_out_0* core to the video signal containing embedded synchronization pulses. This video signal is required by the output HDMI codec on the Avnet HDMI FMC module. This core is developed by UTIA.
- ***axi_interconnect_0*** IP core provides an interconnection between AXI port of the *axi_vdma_0* and AXI high performance port of the Zynq UltraScale+ (its memory controller). This core is a part of the Vivado 2018.3.

2.4 Auxiliary Cores

The video chain needs other auxiliary cores to run (see Figure 1). All of them are available in Vivado 2018.3 Web Pack tool.

- ***fmc_im_i2c*** is an I^2C controller used for configuration HDMI codecs on the Avnet HDMI FMC module. The speed of the I^2C communication is configured to 100 kHz.
- ***clk_gen*** is a hierarchical block including 2 clock generators. The first one generates 150 MHz clock driving AXI streams. The second clock generator is configured to be programmable from the software application, its output clock is used as pixel a clock of the primary video chain. Figure 5 shows the detail of this block.

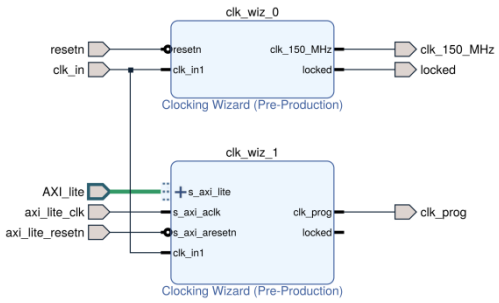


Figure 5: Clock generator.

- ***ps8_0_axi_periph*** IP core provides an interconnection among all AXI-Lite interfaces and Zynq UltraScale+. AXI-lite interface is used for configuring internal registers of IP cores.
- ***rst_sync_to_axi_lite_clk*** and ***rst_sync_to_axis_clk*** cores perform synchronous resets for other cores, *rst_sync_to_axi_lite_clk* is synchronous with 100 MHz clock driving AXI-Lite interfaces, *rst_sync_to_axis_clk* is synchronous with 150 MHz clock driving AXI streams.
- ***zynq_ultra_ps_e_0*** IP core encapsulates complete Zynq UltraScale+ processing system.

3 Required Hardware

The list bellow summarizes required HW components to run the demonstrator.

- Xilinx ZCU102 evaluation board [1]. It uses the Xilinx Zynq UltraScale+ XCZU9EG-2FFVB1156E MPSoC (MultiProcessor System on Chip). The board has 2 GB DDR4 memory. The Zynq UltraScale+ device is quad core ARM A53, dual core ARM Cortex R5 and programmable logic area on a single 16 nm chip (see in Figure 6).

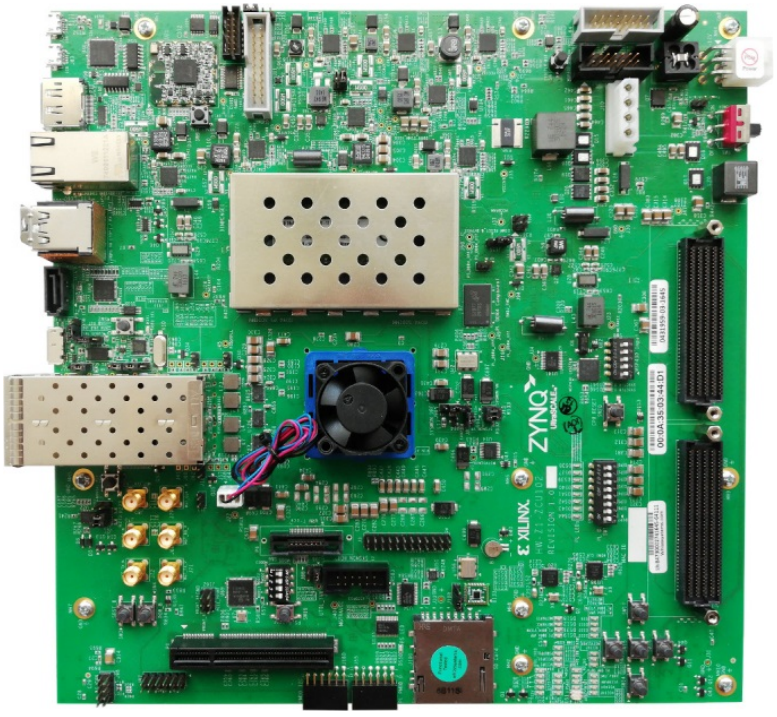


Figure 6: ZCU102 evaluation board [1].

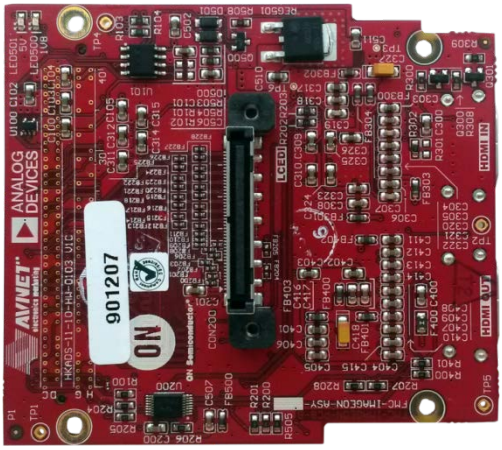


Figure 7: Avnet HDMI Input/Output FMC Module [2][2].

- Avnet HDMI Input/Output FMC Module [2]. It is an expansion board providing HDMI input and HDMI output interfaces in YCrCb 4:2:2 format with embedded synchronization pulses. Figure 7 shows the top view of the FMC card.

4 SW Application

The application uses a serial terminal to communicate with a user. The settings of the terminal are summarized in Table 1. After the application startup is finished and all cores are configured, the application prints its menu on the serial terminal screen. The menu is presented in Table 2.

Table 1: Serial terminal settings.

Parameter	Value
Speed	115200
Data bits	8
Stop bits	1
Parity	None
Control Flow	None

Table 2: Application menu.

Key	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, a	Set output resolution of the primary video chain. Choices: 1920x1080p60, 1920x1200p50, 1600x1200p50, 1680x1050p60, 1280x1024p60, 1280x720p60, 1024x768p60, 800x600p60, 640x480p60, 600x800p60
l	Shift output image of the primary video chain to the left by 4 pixels.
r	Shift output image of the primary video chain to the right by 4 pixels.
d	Shift output image of the primary video chain down by 1 line.
u	Shift output image of the primary video chain up by 1 line.
z	Set the image position to point [0, 0].
m	Print this menu
x	Exit the application

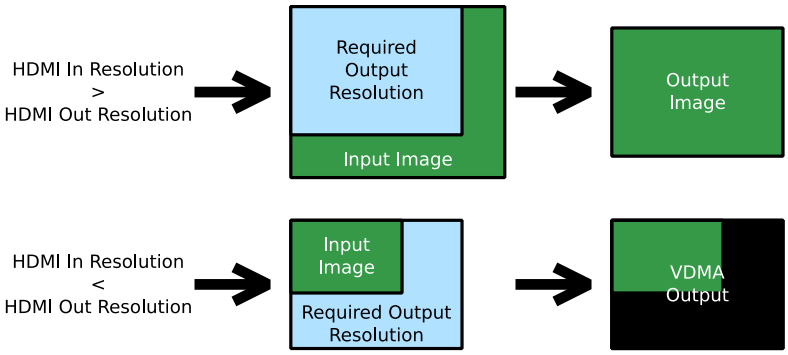


Figure 8: Behavior of the VDMA in the primary video chain demo when the input resolution is not the same as the output resolution.

The application is a video pass through demonstrator. The video signal originates from the HDMI Input on the Avnet FMC module, it is stored in the video frame buffer. After that it is read from the frame buffer and drives to Avnet HDMI Output part of the FMC module. Table 3 summarizes supported input video signal resolutions as they are presented by EDID to the input video signal source (PC graphic card). The output resolution can be changed on the fly, supported resolutions are presented in Table 2. If the resolution of the input video signal is less than the output resolution, the whole input video image will be displayed with additional black frame to comply the output resolution. In case that the resolution of the input video signal is greater than the output resolution, the output will be created by cropping of the input video signal. This behavior is shown in Figure 8. In this case the image can be also shifted to left, to right, up and down.

Table 3: HDMI Input EDID - supported input resolutions.

Resolution	Frame rate
1920x1080, 1680x1050, 1440x900, 1366x768, 1280x1024, 1280x960, 1280x800, 1280x720, 1152x864, 1152x720, 1024x768, 800x600, 800x480, 720x576, 720x480, 640x480	60
1600x1200	50

5 Demonstrator Startup

To run the demonstrator follow the steps bellow.

1. Install Avnet FMC module to the ZCU102 HPC0 FMC connector. HPC1 connector is not completely routed to the Zynq UltraScale device. Therefor it cannot provide a full HDMI input and output functionality of the Avnet FMC module.
2. The ZCU102 board respects the FMC Vita standard. It means that it reads an EEPROM on the FMC module to get information about the plugged card. According to this information, it set a VADJ voltage provided to the board. As the Avnet FMC module does not provide proper values, the VADJ is set to 0 V. To avoid this behavior, it is needed to program the ZCU102 board to set the VADJ voltage always to 1.8 V.
    a. Download *rdf0382* package from Xilinx web page and unpack it. The resultant folder should be named *zcu102_scui*:

    https://www.xilinx.com/member/forms/download/design-license.html?cid=97c50290-ae85-4f71-994b-e5b4216f2a1c&filename=rdf0382-zcu102-system-controller-c-2018-2.zip

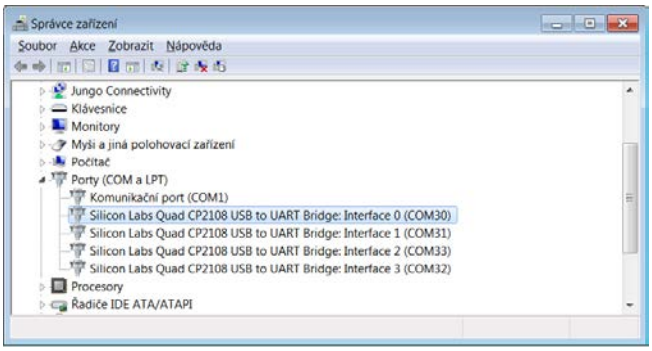
b. Download and install CP210x drivers for Windows

   https://www.silabs.com/products/development-tools/software/usb-to-uart-bridge-vcp-drivers

c. Connect a micro USB cable to USB JTAG on the ZCU102 board.

d. Connect a micro USB cable to USB UART on the ZCU102 board.

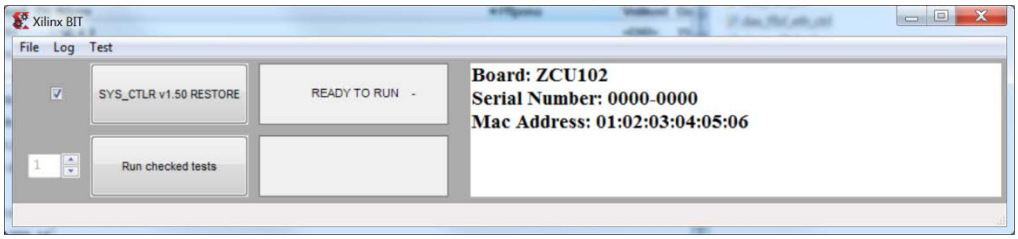
e. Power the board on and get information about version of the *CP210x*.



In our case it is *CP2108*.

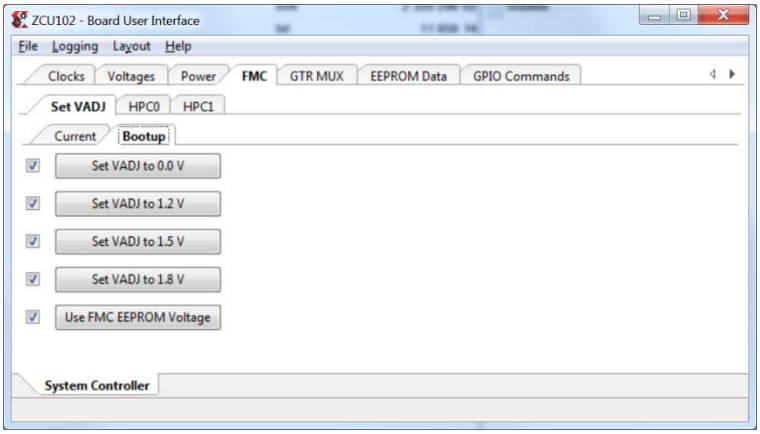
f. In the file *zcu102_scui/flash_restore/tests/ZCU102/bat/firmware_flash_gui_070517.bat* change the string *CP210x* to *CP2108* (use your version).

g. Flash the ZCU102 firmware to the latest version as Xilinx recommends. Run program *zcu102/zcu102_scui/flash_restore/BIT.exe*.



The program asks you for a ZCU102 board serial number and for a MAC address. Both are written on the board. It also asks for a path to the Vivado installation. Click on button *SYS_CTRL v1.50 RESTORE.*

h. Set the board to have VADJ always 1.8 V. Start program *zcu102/zcu102_scui/BoardUI.exe*. It asks for It also asks for a path to the Vivado installation. Go to tab *FMC/Set VADJ/Bootup* and click on *Set VADJ to 1.8 V* button.



i. Switch the ZCU102 board off.

3. Connect the Avnet HDMI output to monitor capable of displaying Full HD resolution at 60 frames per second (1920x1080p60).
4. Connect a valid video signal to the Avnet HDMI input (output from the PC graphic card for instance). Table 3 summarizes all resolutions presented by EDID.
5. Serial terminal settings:
   - Baud rate – 115200
   - Data bits – 8
   - Stop bits – 1
   - Parity – none
   - Flow control – none
6. Copy *BOOT.bin* file to the root of the SD card. The attached package contains two versions of the file, one for ES2 version of the Zynq UltraScale+ and other for the production version of the silicon. See the package content in Section 6.
7. Insert the SD card to the slot on the ZCU102 board.
8. Set SW6 [4:1] to off, off, off, on to enable booting from the SD card.
9. Power the board on (12 V).
10. Observe the serial terminal to see the application prints and to control the demonstrator.

To obtain all demonstrator source codes, do not hesitate to contact UTIA partner at contact e-mails kadlec@utia.cas.cz or kohoutl@utia.cas.cz.

6 Package Content

```
.
├── doc
└── prebuilt
    ├── es2
    │   └── BOOT.bin
    └── production
        └── BOOT.bin
```

7 References

[1] Xilinx, „ZCU102 Evaluation Board User Guide UG1182,“ 11 01 2019. [Online]. Available: https://www.xilinx.com/support/documentation/boards_and_kits/zcu102/ug1182-zcu102-eval-bd.pdf.

[2] AVNET, „HDMI Input/Output FMC Module,“ 11 04 2019 [Online]. Available: https://www.avnet.com/shop/us/products/avnet-engineering-services/aes-fmc-hdmi-cam-g-3074457345635221625/.