Application Note

ÚTIA Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

Support for TE0820 modules with Vitis AI 3.0 DPU

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Revision history

Rev.	Date	Author	Description
v01	1.2.2024	J.K	Initial release
v02	2.2.2024	J.K	Manual creation of extensible platform
v03	20.2.2024	J.K	Added fast track script

Contents

Acknowledgement

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https://zs.utia.cas.cz/index.php?ids=projects/eecone

https://eecone.com/eecone/home/

1 Introduction

EECONE project *https://eecone.com/eecone/home/* work package 4, task 4.3 is investigating measures to support second life of electronics due to modular design.

Work package 4 task 4.4 is investigating measures to support extension of life of electronics due to methodology of support used custom platform to adapt for the in-time-evolving design tools and embedded Linux PetaLinux operating system.

UTIA AV CR, v.v.i. (Institute of Information Theory and Automation of the Czech Academy of Sciences, in short UTIA) is not-for profit research institute located in Prague, Czech Republic. UTIA is involved as partner in both tasks, T4.3 and T4.4.

Both EECONE task require specification of comparable reference systems which are based on modular HW with potential for “second life” by reuse of modules or use cost optimized PCB HW without modularity.

Systems (with HW modularity or low cost single PCB) should be capable to perform similar challenging tasks. Systems have to be capable to accelerate in HW AI inference algorithms with video camera input for edge application like person detection, face detection, car-make or car-type detection and graphical output to local display or to the remote PC connected by wired Ethernet in a local network.

Systems should also support remote monitoring and control from remote PC connected by wired Ethernet in a local network.

The investigated measures and methodologies to support “second life” of electronic modules (T4.3) and measures to support extension of life of electronics (T4.4) due to methodology of support used custom platform to adapt for the in-time-evolving design tools and embedded Linux PetaLinux operating system. We target developers designing the final commercial, AI inference based edge applications, mainly in the area of home automation.

Based on these requirements UTIA have selected two types of systems:
- Low cost systems. See [2], [3]
- Modul based systems. See [4] and [5]. [5] is this application note.

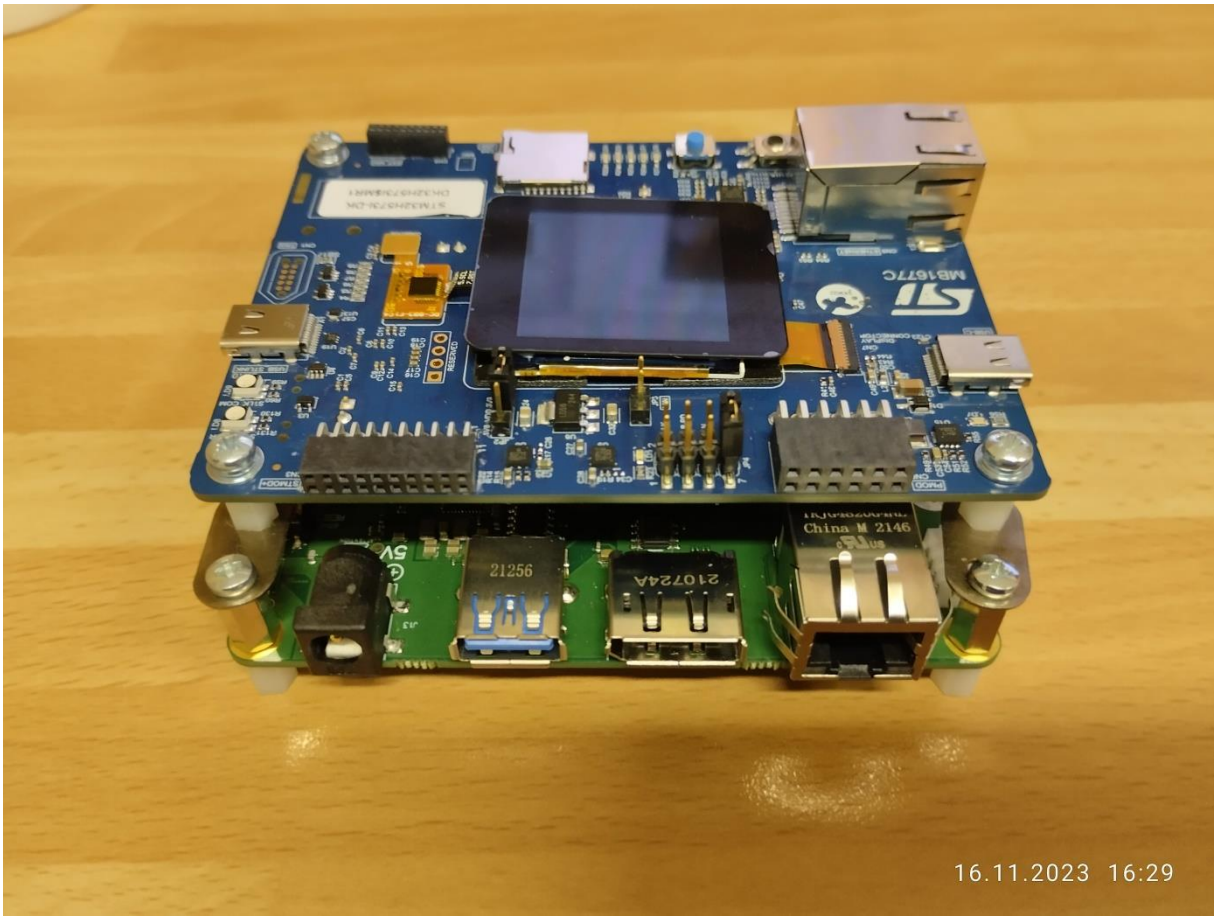
Both compared types of systems use STMicroelectronic STM32H573I-DK board for:
- local system control on small graphical touch screen display
- remote system control from www browser based on www-server or secure communication based on mqtt client. Board is supported by STMicroelectronic CubeMX SW framework and also by NetXDuo SW framework on top of ThreadX OS and FileX SW package.

The MCU used on STM32H573I-DK board is a 40nm chip with 32 bit ARM M33 MCU operating with 250 MHz clock, 2 MBytes of program flash memory and 640 KBytes of RAM.

Compared systems use 16nm AMD ZynqUltrascale+ device with 64 bit ARM A53 Microprocessor and programmable logic in the same device and Petalinux OS.
- Low-cost systems have an AMD ZynqUltrascale+ device and DDR4 with all peripheral interfaces soldered on a single, low cost PCB
- Module-based systems have an AMD ZynqUltrascale+ device and DDR4 soldered on an 4x5 cm module connected by connectors to a carrier board with all peripheral interfaces

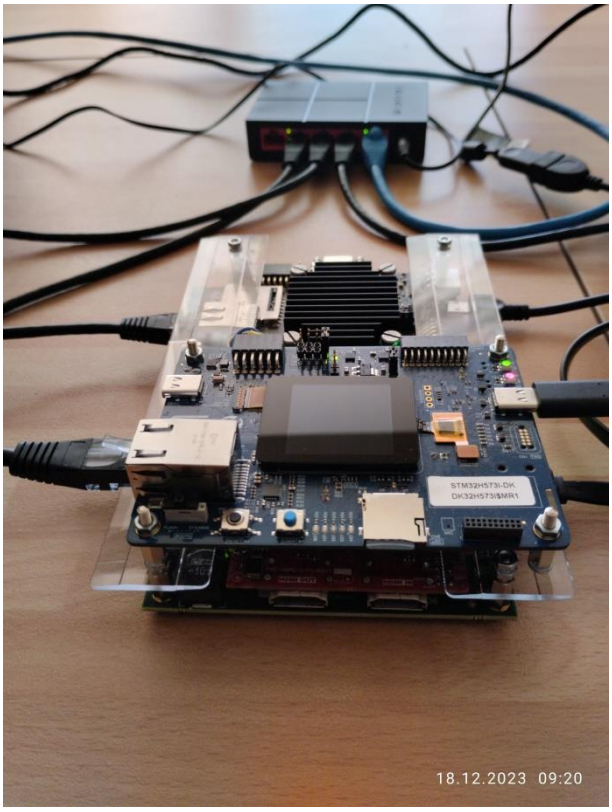
1.1 Low cost systems used by UTIA in EECONE T4.3 and T4.4

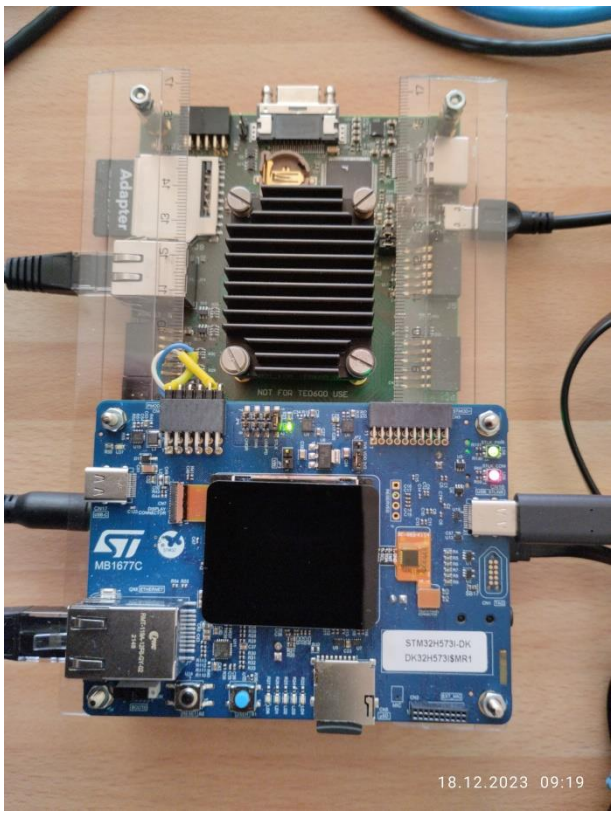
[1]	STM32H573I-DK	https://www.st.com/en/evaluation-tools/stm32h573i-dk.html	Local or remote system control (www-server or secure mqtt client) for [2], [3]
[2]	TE0802-02-1BEV2-A	https://shop.trenz-electronic.de/en/TE0802-02-1BEV2-A-MPSoC-Development-Board-with-AMD-Zynq-UltraScale-ZU1EG-and-1-GB-LPDDR4?c=474	AMD Vitis AI 3.0 AMD DPU in PL USB camera, remote X11 desktop
[3]	TE0802-02-2AEV2-A	MPSoC Development Board mit AMD Zynq™ UltraScale+™ ZU2 und 1 GB LPDDR4 | Trenz Electronic GmbH Online Shop (EN) (trenz-electronic.de)	AMD Vitis AI 3.0 AMD DPU in PL USB camera, remote X11 desktop



1.2 Module based systems used by UTIA in EECONE T4.3 and T4.4

[1]	STM32H573I-DK TE0701-06 Carrier Board for Trenz Electronic 4 x 5 Modules TE0821 or TE0820	https://www.st.com/en/evaluation-tools/stm32h573i-dk.html https://shop.trenz-electronic.de/en/TE0701-06-Carrier-Board-for-Trenz-Electronic-4-x-5-Modules?c=261	Local or remote system control (www-server or secure mqtt client) for 2-1, 2-2 Carrier Board for range of 4x5 cm modules [3], [4].
[4]	TE0821 Module: **17 module types** (to be supported)	https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/TE08XX-Zynq-UltraScale/TE0821-Zynq-UltraScale/	AMD Vitis AI 3.0 AMD DPU in PL USB camera remote X11 desktop
[5]	TE0820 Module: **100 module types** (to be supported)	https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/TE08XX-Zynq-UltraScale/TE0821-Zynq-UltraScale/	AMD Vitis AI 3.0 AMD DPU in PL USB camera remote X11 desktop





This application note [5] and the accompanying evaluation package describe support for systems based on TE0820 modules. It is available for free public download from UTIA server dedicated to UTIA contributions to EECONE project:
https://zs.utia.cas.cz/index.php?ids=projects/eecone

It will be also available for free public download in format of an wiki tutorial on Trenz Electronic wiki server:
https://wiki.trenz-electronic.de/display/PD/Vitis+AI+and+Vitis+Acceleration+Tutorials+with+Trenz+Electronic+Modules

1.3 Objective of This Application Note and Evaluation Package

This application note and the accompanying evaluation package describe system [**5].**

This application note describes how to design custom HW platform with AMD DPU for Vitis 2022.2 AI 3.0 inference for family of Trenz Electronic modules TE0820 with AMD Zynq Ultrascale+ device.

This application note [5] is using AMD Vitis 2022.2 and PetaLinux 2022 tools installed on Ubuntu 20.04. The described configuration integrated AMD DPU IP, version v4.1.0, with architecture DPUCZDX8G.

Described board configuration can operate as small standalone computer with 1 Gb Ethernet connectivity, and remote X11 desktop. Support package for this application note will be available for public download from [5].

The installed AMD DPU configurations require recompilation of Vitis AI 3.0 examples and inference models in the Vitis AI framework. This compilation process will be described in separate application note [6].

This application supports family of TE0820 modules listed in next tables with ID 15 to 115.

Process will be demonstrated on these two TE0820 module examples:

- ID=84 module: TE0820-05-4DE21MA, device xczu4ev-sfvc784-1-e, 2GB DDR4
- ID=106 module: TE0820-05-2AE21MA, device xczu2cg-sfvc784-1-e, 2GB DDR4

Module TE0820-05-4DE21MA has four A53 ARM cores and contains Bram and also URAM blocks in the PL part of the device. Therefore, it is possible to implement all possible configurations of the AMD DPU (from B512 up to B4096) in PL. Implementaton of B4096 is demonstrated. Module requires integration on carrier board TE0701-06 due to higher requirements DC/DC converters.

Module TE0820-05-2AE21MA has only two A53 ARM cores and contains only BRAM blocks in relatively small PL part of the device. Therefore, it is possible to implement configuration of the AMD DPU from B512 to B1024. Implementaton of B1024 is demonstrated. This module has signoficantly lower power consumption in comparison to TE0820-05-4DE21MA and allows integration on carrier board TE0701-06 or carrier board TE0707-02. It is compact carrier board with limited DC/DC capabilities.

Specification for each module ID defined in `TE0820_board_files.csv` file is input to the Vivado 2022.2 HW bring-up scripts. It is provided by the company Trenz Electronic. It is part

of package provided by Trenz Electronic for supported family of modules TE0820 for AMD Vivado 2022.2 design flows.

List of supported TE0820 modules is reprinted from `TE0820_board_files.csv` file included in the evaluation package associated to this application note.

This application note and associated evaluation package enables support for “second-life” of **100** types of TE0820.

A module from this mighed has been used originally in another context which might become obsolete. We provide support to reuse this module again in large and challenging range of Vitis AI 3.0 HW accelerated inference applications.

ID	PRODID	PARTNAME	BOARDNAME	SHORTNAME	ZYNQFLASHTYP	FPGAFLASHTYP	PCB_REV	DDR_SIZE	FLASH_SIZE	EMMC_SIZE
15	TE0820-03-04EV-1EA	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
16	TE0820-03-02CG-1EA	xczu2cg-sfvc784-1-e	trenz.biz:te0820_2cg_1e:part0:2.0	2cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
17	TE0820-03-02EG-1EA	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
18	TE0820-03-02EG-1EL	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
19	TE0820-03-03CG-1EA	xczu3cg-sfvc784-1-e	trenz.biz:te0820_3cg_1e:part0:2.0	3cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
20	TE0820-03-04CG-1EA	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
21	TE0820-03-03EG-1EA	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
22	TE0820-03-03EG-1EL	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	4GB
23	TE0820-03-2AI21FA	xczu2cg-sfvc784-1-i	trenz.biz:te0820_2cg_1i:part0:2.0	2cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
24	TE0820-03-2BE21FL	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
25	TE0820-03-3AI210A	xczu3cg-sfvc784-1-i	trenz.biz:te0820_3cg_1i:part0:2.0	3cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	0GB
26	TE0820-03-3BE21FA	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
27	TE0820-03-3BE21FL	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
28	TE0820-03-02CG-1ED	xczu2cg-sfvc784-1-e	trenz.biz:te0820_2cg_1e:part0:2.0	2cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
29	TE0820-03-2AE21FA	xczu2cg-sfvc784-1-e	trenz.biz:te0820_2cg_1e:part0:2.0	2cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
30	TE0820-03-2BE21FA	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
31	TE0820-03-3AE21FA	xczu3cg-sfvc784-1-e	trenz.biz:te0820_3cg_1e:part0:2.0	3cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
32	TE0820-03-3AI21FA	xczu3cg-sfvc784-1-i	trenz.biz:te0820_3cg_1i:part0:2.0	3cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
33	TE0820-03-4AE21FA	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
34	TE0820-03-4DE21FA	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
35	TE0820-03-4DI21FA	xczu4ev-sfvc784-1-i	trenz.biz:te0820_4ev_1i:part0:2.0	4ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
36	TE0820-03-4DE21FL	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
37	TE0820-03-4DE21FC	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
38	TE0820-03-4AI21FI	xczu4cg-sfvc784-1-i	trenz.biz:te0820_4cg_1i:part0:3.0	4cg_1i_x_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
39	TE0820-03-5DR21FA	xazu5ev-sfvc784-1Q-q	trenz.biz:te0820_5ev_1q:part0:2.0	5ev_1q_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
40	TE0820-03-2BI21FA	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
41	TE0820-03-2BI21FL	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
42	TE0820-03-5DI21FA	xczu5ev-sfvc784-1-i	trenz.biz:te0820_5ev_1i:part0:2.0	5ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV03	2GB	128MB	8GB
43	TE0820-04-2AE21FA	xczu2cg-sfvc784-1-e	trenz.biz:te0820_2cg_1e:part0:2.0	2cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
44	TE0820-04-2AI21FA	xczu2cg-sfvc784-1-i	trenz.biz:te0820_2cg_1i:part0:2.0	2cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
45	TE0820-04-2BE21FA	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
46	TE0820-04-2BE21FAJ	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
47	TE0820-04-2BE21FL	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
48	TE0820-04-2BE21-V1	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
49	TE0820-04-2BI21FA	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
50	TE0820-04-2BI21FL	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
51	TE0820-04-3AE21FA	xczu3cg-sfvc784-1-e	trenz.biz:te0820_3cg_1e:part0:2.0	3cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
52	TE0820-04-3AI21FA	xczu3cg-sfvc784-1-i	trenz.biz:te0820_3cg_1i:part0:2.0	3cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
53	TE0820-04-3AI21FAT	xczu3cg-sfvc784-1-i	trenz.biz:te0820_3cg_1i:part0:2.0	3cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
54	TE0820-04-3BE21FA	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
55	TE0820-04-3BE21FL	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
56	TE0820-04-3BE21KA	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	64GB
57	TE0820-04-4AE21FA	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
58	TE0820-04-4AI21FI	xczu4cg-sfvc784-1-i	trenz.biz:te0820_4cg_1i:part0:3.0	4cg_1i_x_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
59	TE0820-04-4BI21KL	xczu4eg-sfvc784-1-i	trenz.biz:te0820_4eg_1i:part0:2.0	4eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	64GB
60	TE0820-04-4DE21FA	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB

ID	PRODID	PARTNAME	BOARDNAME	SHORTNAME	ZYNQFLASHTYP	FPGAFLASHTYP	PCB_REV	DDR_SIZE	FLASH_SIZE	EMMC_SIZE
61	TE0820-04-4DE21FL	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
62	TE0820-04-4DI21FA	xczu4ev-sfvc784-1-i	trenz.biz:te0820_4ev_1i:part0:2.0	4ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
63	TE0820-04-5DI21FA	xczu5ev-sfvc784-1-i	trenz.biz:te0820_5ev_1i:part0:2.0	5ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
64	TE0820-04-5DR21FA	xazu5ev-sfvc784-1Q-q	trenz.biz:te0820_5ev_1q:part0:2.0	5ev_1q_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
65	TE0820-04-3BE21ML	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
66	TE0820-04-4DE21MA	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
67	TE0820-04-4DI21MA	xczu4ev-sfvc784-1-i	trenz.biz:te0820_4ev_1i:part0:2.0	4ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
68	TE0820-04-S002	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
69	TE0820-04-S005	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
70	TE0820-04-S004	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
71	TE0820-04-2BE21MA	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
72	TE0820-04-S006	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
73	TE0820-04-2BI21ML	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
74	TE0820-04-S002C1	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
75	TE0820-04-S003	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
76	TE0820-04-S009	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
77	TE0820-04-S010	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
78	TE0820-04-4AE21MA	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
79	TE0820-04-2BE21MAJ	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
80	TE0820-04-3BE21MLZ	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
81	TE0820-04-S013	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
82	TE0820-04-S016	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
83	TE0820-05-4BI21PLZ	xczu4eg-sfvc784-1-i	trenz.biz:te0820_4eg_1i:part0:2.0	4eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	64GB
84	TE0820-05-4DE21MA	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
85	TE0820-05-S002C1	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
86	TE0820-05-S003	xczu4ev-sfvc784-1-e	trenz.biz:te0820_4ev_1e:part0:2.0	4ev_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
87	TE0820-05-S004C1	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
88	TE0820-05-S008C1	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
89	TE0820-04-S018	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
90	TE0820-05-2AE21MAZ	xczu2cg-sfvc784-1-e	trenz.biz:te0820_2cg_1e:part0:2.0	2cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
91	TE0820-05-3BE21MAZ	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
92	TE0820-05-S014C1	xczu4cg-sfvc784-1-e	trenz.biz:te0820_4cg_1e:part0:2.0	4cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
93	TE0820-04-5DI21MA	xczu5ev-sfvc784-1-i	trenz.biz:te0820_5ev_1i:part0:2.0	5ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
94	TE0820-05-4BI21PL	xczu4eg-sfvc784-1-i	trenz.biz:te0820_4eg_1i:part0:2.0	4eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	64GB
95	TE0820-05-S016	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
96	TE0820-04-2BI21MA	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
97	TE0820-05-3BE21MA	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
98	TE0820-05-S013	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
99	TE0820-05-2AI81MA	xczu2cg-sfvc784-1-i	trenz.biz:te0820_2cg_1i:part0:2.0	2cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
100	TE0820-05-3BI21ML	xczu3eg-sfvc784-1-i	trenz.biz:te0820_3eg_1i:part0:2.0	3eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
101	TE0820-04-2AI21MC	xczu2cg-sfvc784-1-i	trenz.biz:te0820_2cg_1i:part0:2.0	2cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV04	2GB	128MB	8GB
102	TE0820-05-2BI81ML	xczu2eg-sfvc784-1-i	trenz.biz:te0820_2eg_1i:part0:2.0	2eg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
103	TE0820-05-S022	xczu3cg-sfvc784-1-e	trenz.biz:te0820_3cg_1e:part0:2.0	3cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
104	TE0820-05-2BE21MA	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
105	TE0820-05-4AI21MI	xczu4cg-sfvc784-1-i	trenz.biz:te0820_4cg_1i:part0:3.0	4cg_1i_x_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
106	TE0820-05-2AE21MA	xczu2cg-sfvc784-1-e	trenz.biz:te0820_2cg_1e:part0:2.0	2cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
107	TE0820-05-2AI21MA	xczu2cg-sfvc784-1-i	trenz.biz:te0820_2cg_1i:part0:2.0	2cg_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
108	TE0820-05-2BE21MAJ	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
109	TE0820-05-3AE21MA	xczu3cg-sfvc784-1-e	trenz.biz:te0820_3cg_1e:part0:2.0	3cg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
110	TE0820-05-3BE81ML	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
111	TE0820-05-4DI21MA	xczu4ev-sfvc784-1-i	trenz.biz:te0820_4ev_1i:part0:2.0	4ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
112	TE0820-05-5DI81MA	xczu5ev-sfvc784-1-i	trenz.biz:te0820_5ev_1i:part0:2.0	5ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
113	TE0820-05-S017C1	xczu2eg-sfvc784-1-e	trenz.biz:te0820_2eg_1e:part0:2.0	2eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
114	TE0820-05-S020	xczu3eg-sfvc784-1-e	trenz.biz:te0820_3eg_1e:part0:2.0	3eg_1e_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB
115	TE0820-05-5DI21MA	xczu5ev-sfvc784-1-i	trenz.biz:te0820_5ev_1i:part0:2.0	5ev_1i_2gb	qspi-x8-dual_parallel	mt25qu512-qspi-x8-dual_parallel	REV05	2GB	128MB	8GB

Supported TE0820 modules with ID = 15 ... 115

2 Prepare Reference Design for Extensible Custom Platform

The design proces is demonstrated for module with ID=84: TE0820-05-4DE21MA, device xczu4ev-sfvc784-1-e, 2GB DDR4. If your module has different ID, replace 84 with that ID.

In Ubuntu terminal, source paths to Vitis and Vivado tools by

```
$ source /tools/Xilinx/Vitis/2022.2/settings64.sh
```

Download TE0820 test_board Linux Design file(see Reference Design download link on chapter Requirements) with pre-build files to

```
~/Downloads/TE0820-test_board-vivado_2022.2-build_2_20230622121437.zip
```

This TE0820 test_board ZIP file contains bring-up scripts for creation of Petalinux for range of modules in zipped directory named “test_board”.

Unzip the file to directory:

```
~/work/te0820_84_240
```

All supported modules are identified in file:

```
~/work/te0820_84_240/test_board/board_files/TE0820_board_files.csv
```

We will select module 84 with name TE0820-05-4DE21MA, with device xczu04ev-sfvc784-1-e on TE0701-06 carrier board. We will use default clock 240 MHz. That is why we name the package te0820_84_240 and proposed to unzip the TE0820 test_board Linux Design files into the directory:

```
~/work/te0820_84_240
```

2.1 Reference HW for TE0820 module

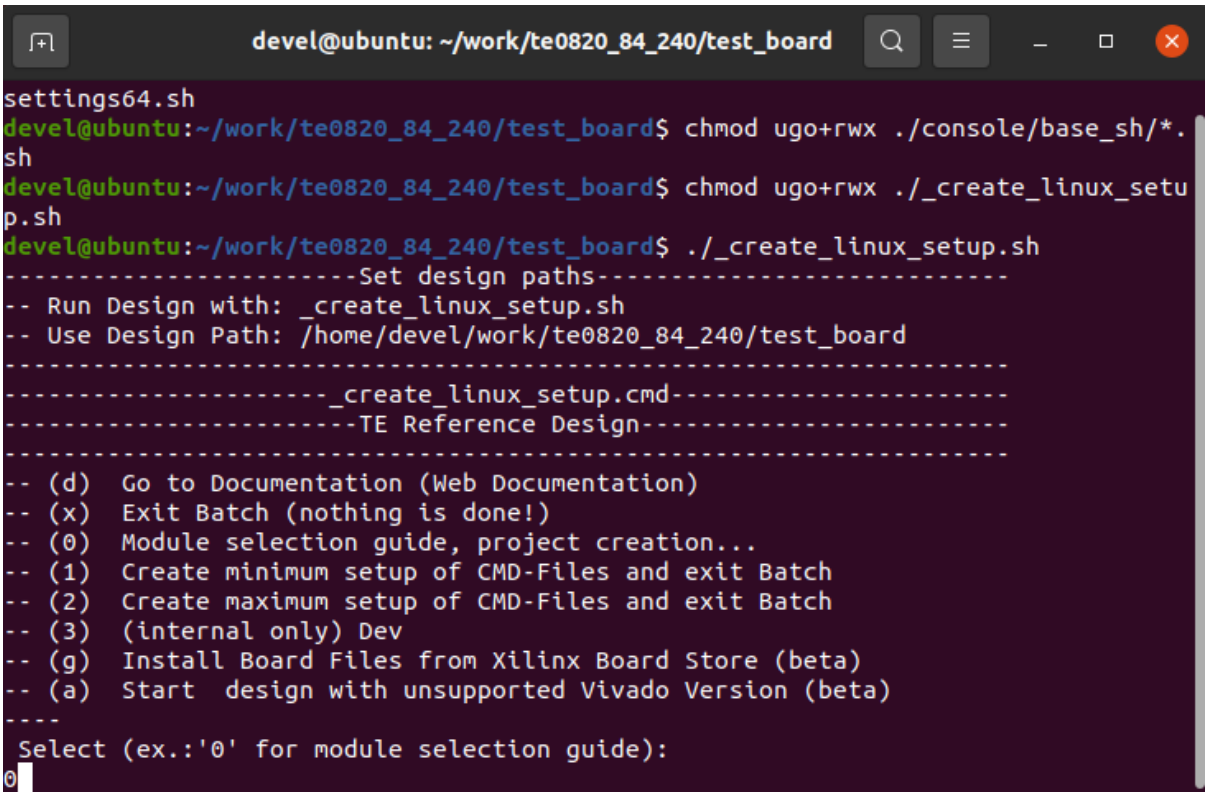
In Ubuntu terminal, change directory to the test_board directory:

```
$ cd ~/work/te0820_84_240/test_board
```

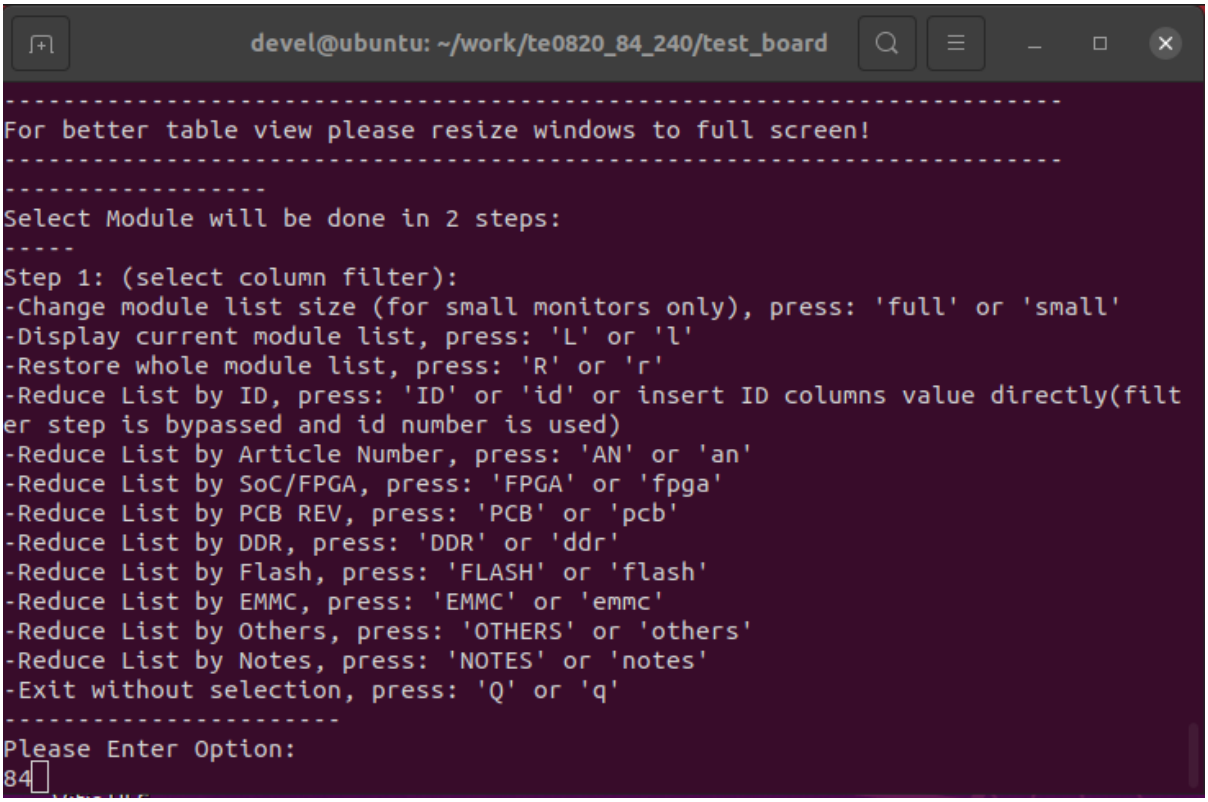
Setup the test_board directory files for a Linux host machine.
In Ubuntu terminal, execute:

```
$ chmod ugo+rwx ./console/base_sh/*.sh

$ chmod ugo+rwx ./_create_linux_setup.sh

$ ./_create_linux_setup.sh
```

Select option (0) to open Selection Guide and press Enter



Select variant 84 from the selection guide, press enter and agree selection



Create Vivado Project with option 1

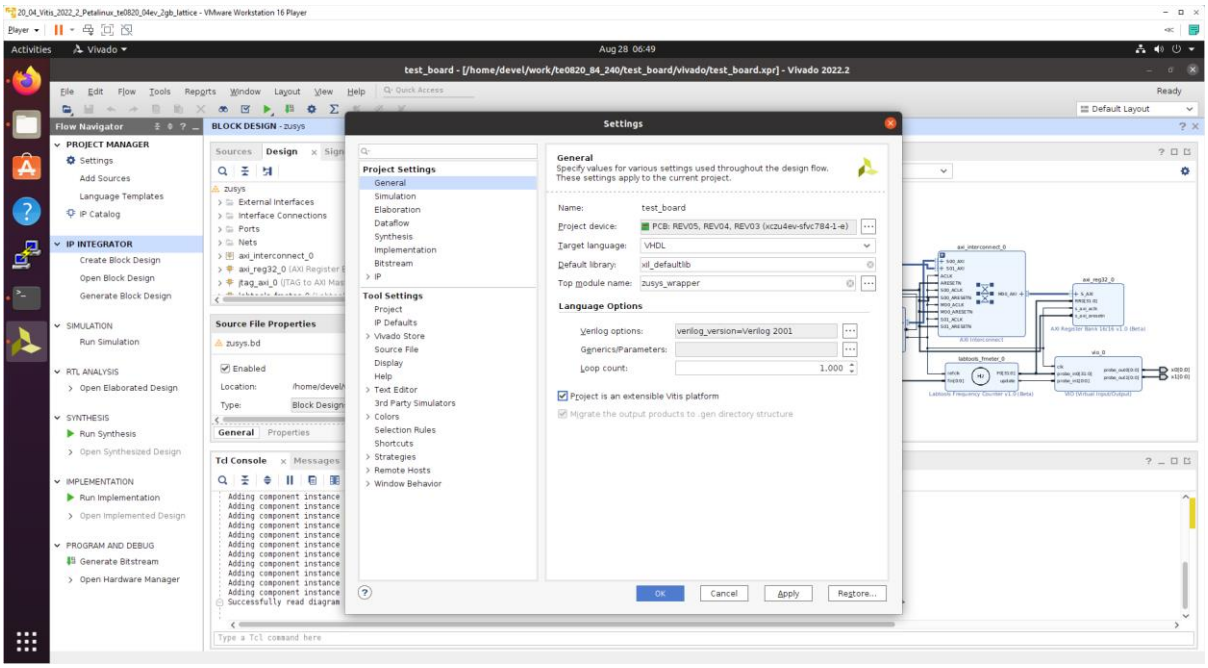
Vivado Project will be generated for the selected variant.

3 HW support for Vitis Extensible Design Flow

3.1 Create Extensible platform HW

This section describes manual creation of extensible platform HW. You can follow it or you can alternatively use the fast track script described in section 3.2.

In Vivado project, click in **Flow Navigator** on **Settings**. In opened Settings window, select **General** in **Project Settings**, select **Project is an extensible Vitis platform**. Click on **OK**.



IP Integrator of project set up as an extensible Vitis platform has an additional Platform Setup window.

Add multiple clocks and processor system reset IPs

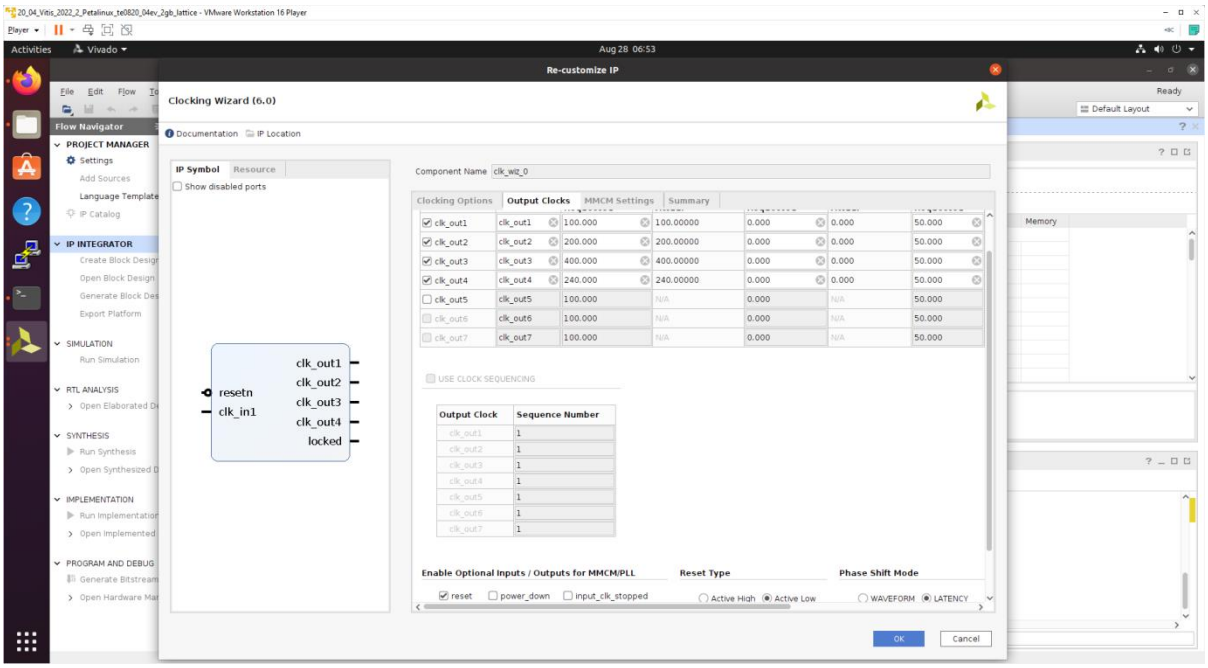
In IP Integrator Diagram Window, right click, select **Add IP** and add **Clocking Wizard** IP **clk_wiz_0**. Double-click on the IP to Re-customize IP window. Select Output Clocks panel. Select four clocks with frequency 100, 200, 400 and 240 MHz.

100 MHz clock will serve as low speed clock.

200 MHz and 400 MHz clock will serve as clock for AMD DPU AI 3.0 HW IP.

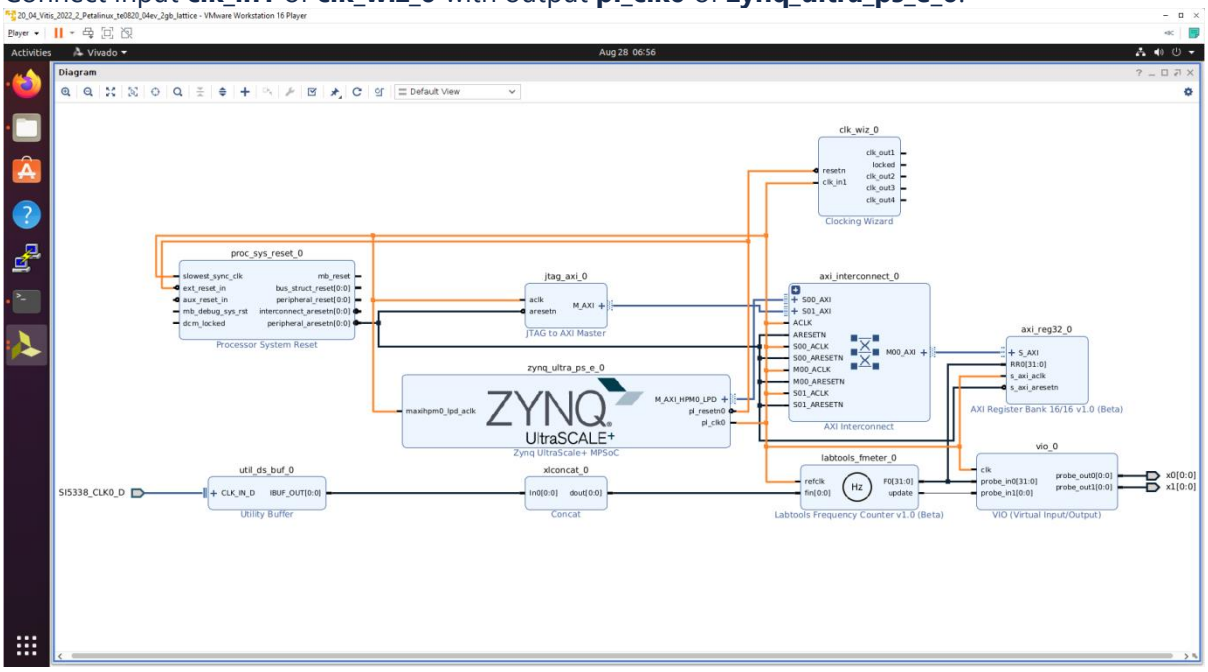
240 MHz clock will serve as the default extensible platform clock. By default, Vitis will compile HW IPs with this default clock.

Set reset type from the default Active High to **Active Low**.

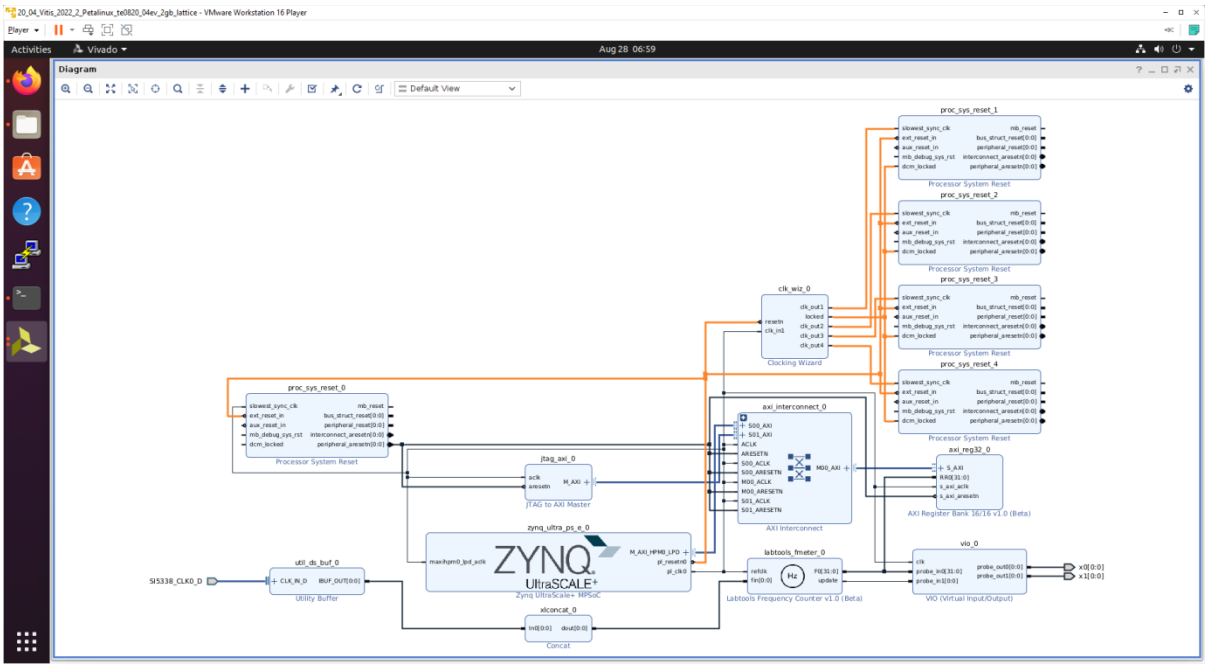


Clik on OK to close the Re-customize IP window.

Connect input **resetn** of **clk_wiz_0** with output **pl_resetn0** of **zynq_ultra_ps_e_0.**
Connect input **clk_in1** of **clk_wiz_0** with output **pl_clk0** of **zynq_ultra_ps_e_0**.



Add and connect four Processor System Reset blocks for each generated clock.

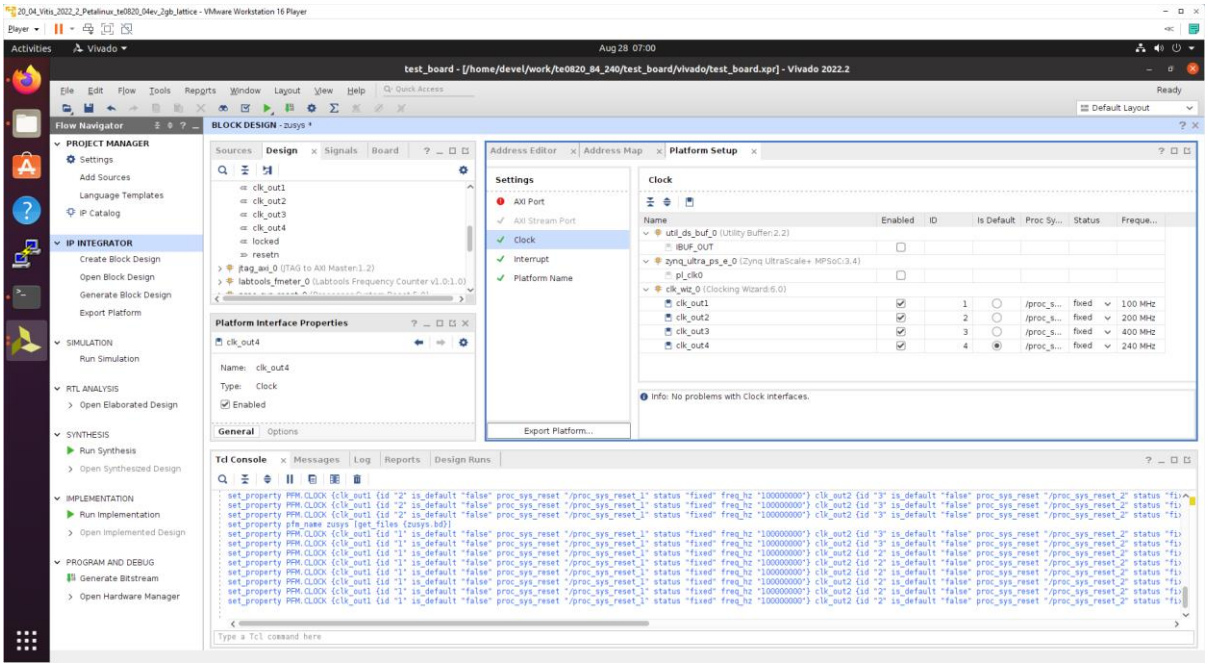


Open **Platform Setup** window of IP Integrator to define Clocks. In **Settings**, select **Clock**.

In “Enabled” column select all four defined clocks **clk_out1**, **clk_out2**, **clk_out3**, **clk_out4** of **clk_wiz_0** block.

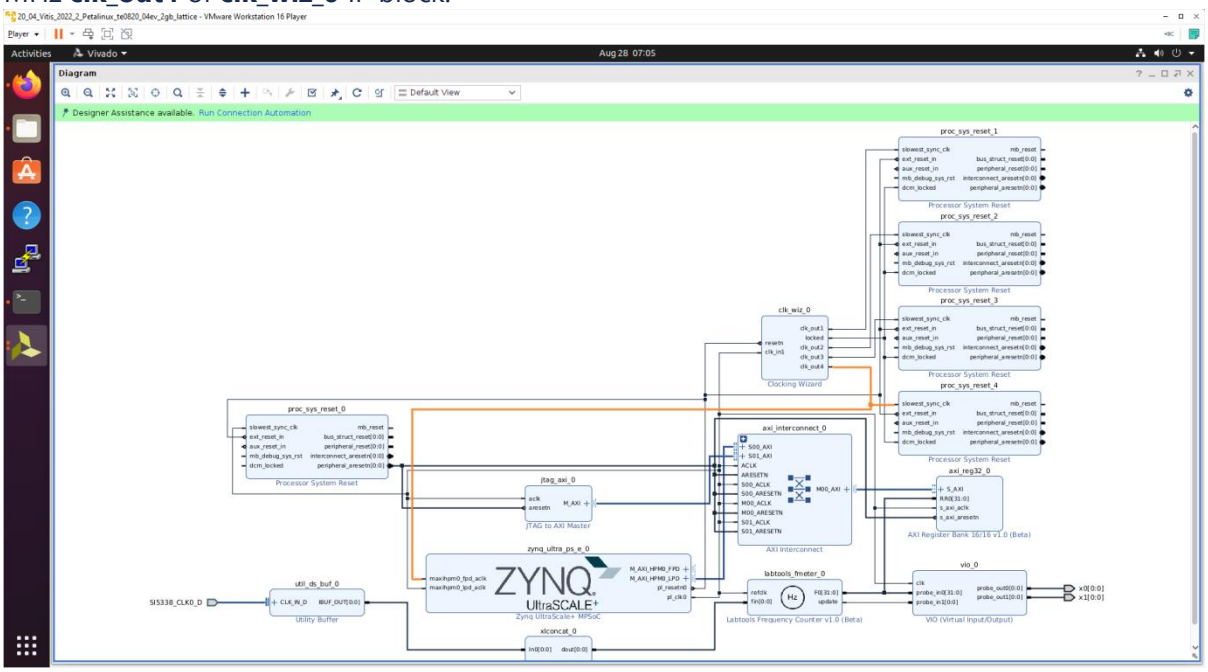
In “ID” column keep the default Clock ID: **1, 2, 3, 4**

In “Is Default” column, select **clk_out4** (with ID=4) as the default clock. One and only one clock must be selected as default clock.



Double-click on **zynq_ultra_ps_e_0** block and enable **M_AXI_HPM0_FPD** port. Select data width 32bit. It will be used for integration of inerrupt controller on new dedicated AXI stream subsystem with 240 MHz clock. It will also enable new input pin **maxihpm0_fpd_aclk** of **zynq_ultra_ps_e_0.** Connect it to 240 MHz clock net.

Connect input pin **maxihpm0_fpd_aclk** of **zynq_ultra_ps_e_0** to the 240 MHz **clk_out4** of **clk_wiz_0** IP block.

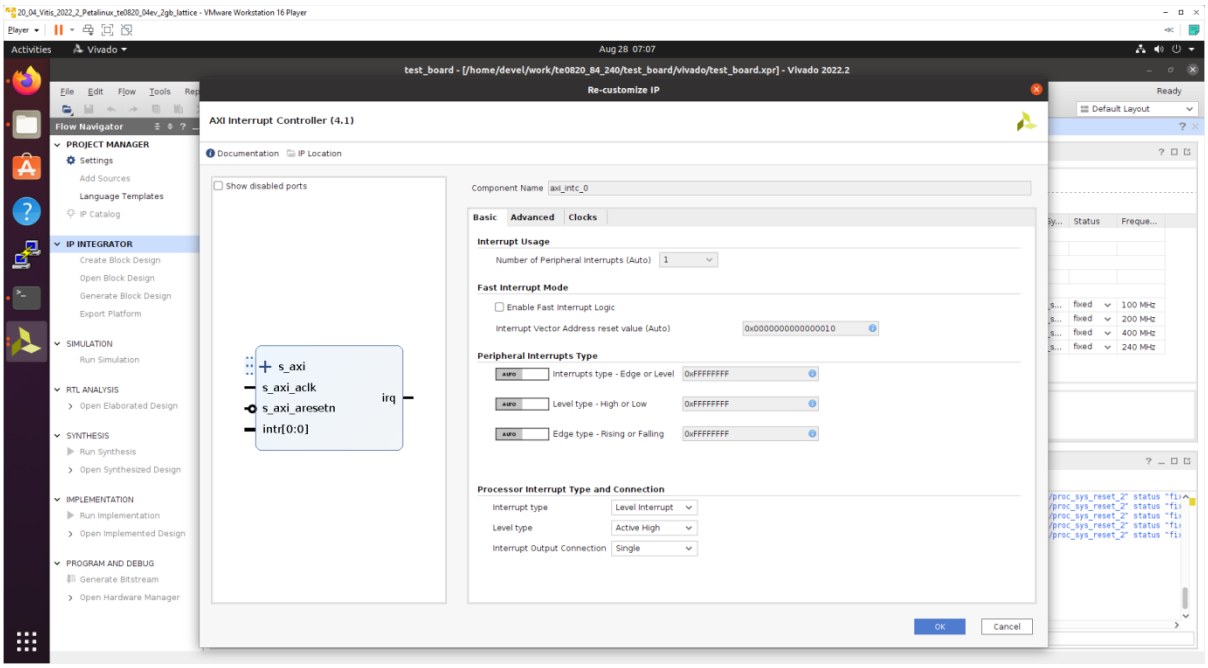


Add, customize and connect the AXI Interrupt Controller

Add AXI Interrupt Controller IP **axi_intc_0**.
Double-click on **axi_intc_0** to re-customize it.

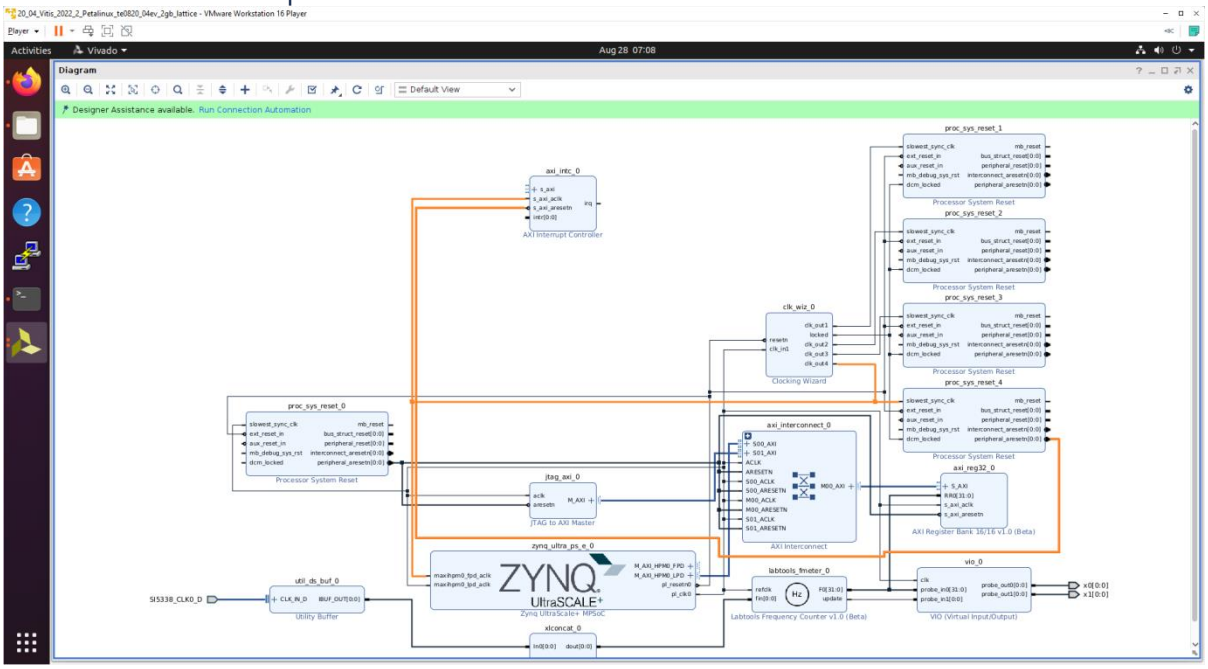
In “Processor Interrupt Type and Connection” section select the “Interrupt Output Connection” from “Bus” to “Single”.

Click on OK to accept these changes.

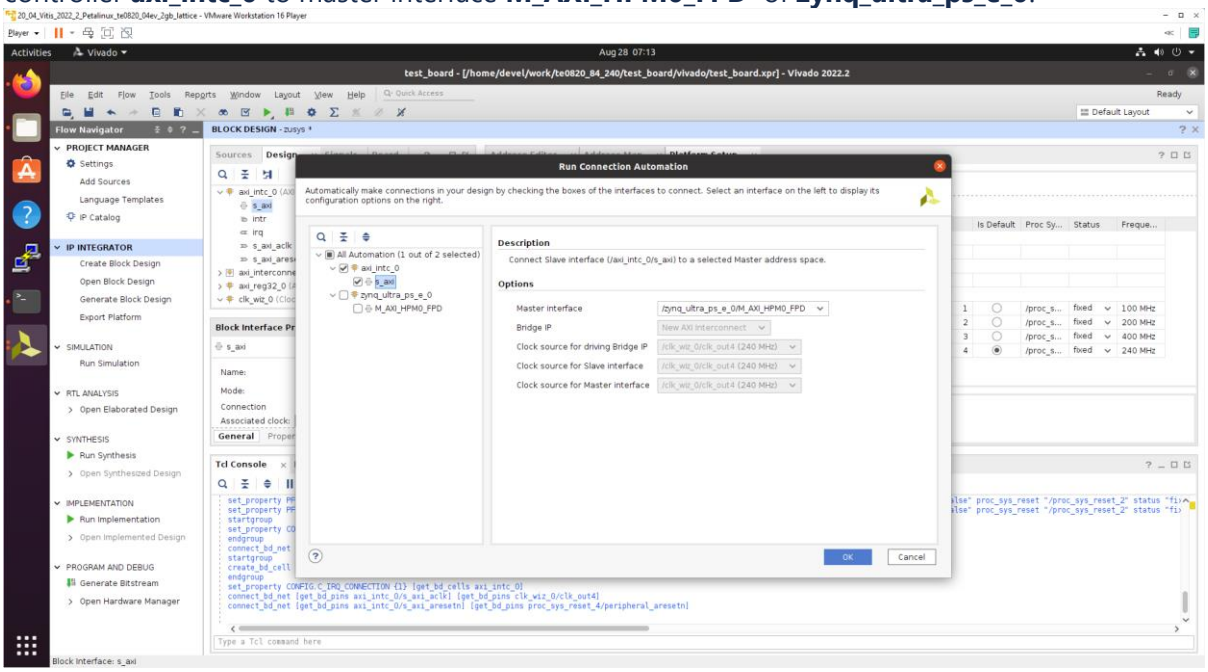


Connect interrupt controller clock input **s_axi_aclk** of **axi_intc_0** to output **dlk_out4** of **clk_wiz_0**. It is the default, 240 MHz clock of the extensible platform.

Connect interrupt controller input **s_axi_aresetn** of **axi_intc_0** to output **peripheral_aresetn[0:0]** of **proc_sys_reset_4** . It is the reset block for default, 240 MHz clock of the extensible platform.

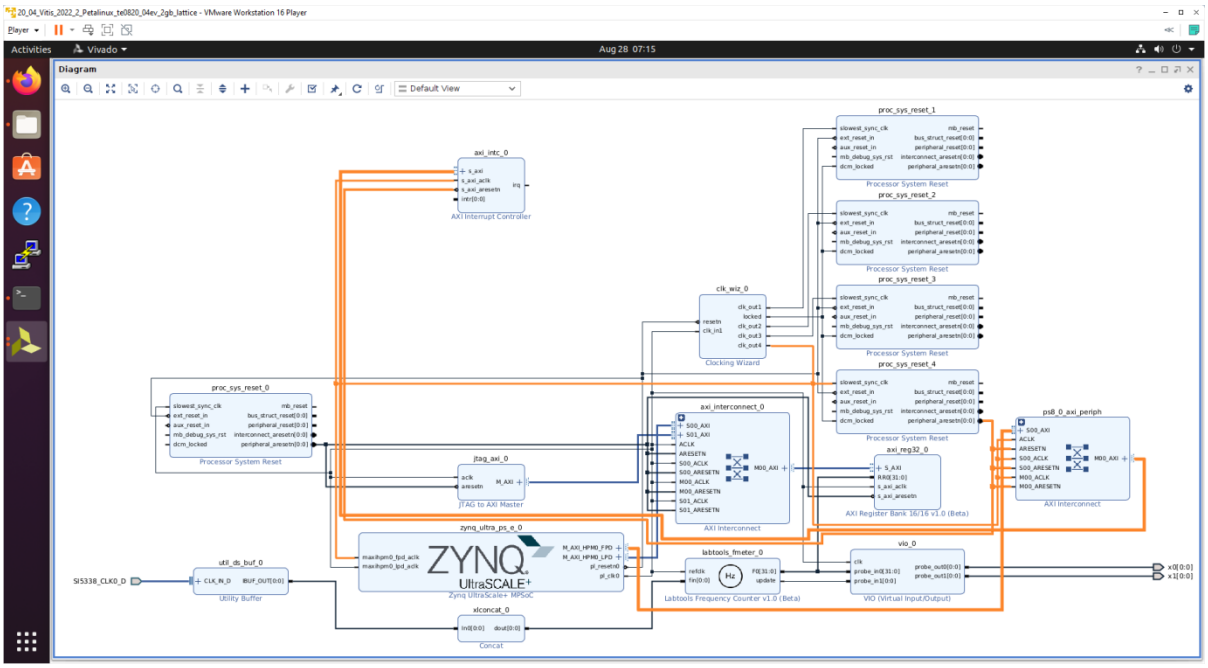


Use the **Run Connection Automation** wizard to connect the axi lite interface of interrupt controller **axi_intc_0** to master interface **M_AXI_HPM0_FPD** of **zynq_ultra_ps_e_0**.

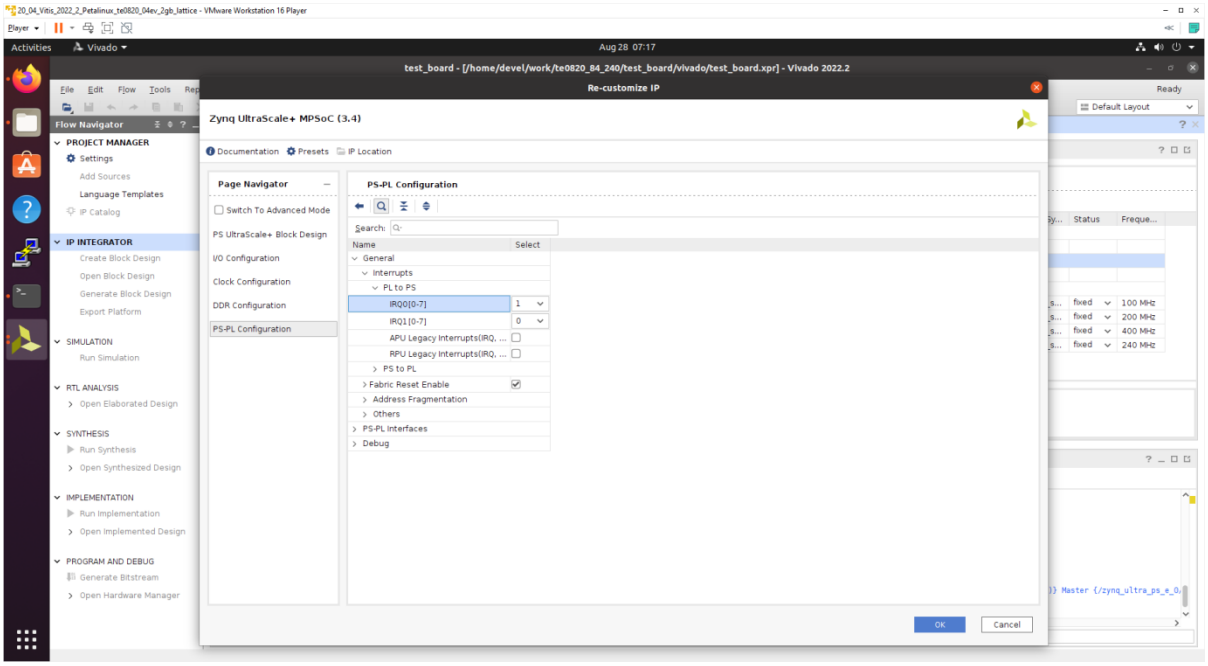


In Run Connection Automaton window, click **OK**.

New AXI interconnect **ps_8_axi_periph** is created. It connects master interface **M_AXI_HPM0_FPD** of **zynq_ultra_ps_e_0** with interrupt controller **axi_intc_0**.



Double-click on **zynq_ultra_ps_e_0** to re-customize it by enabling of an interrupt input **pl_ps_irq0[0:0]**. Click OK.



Modify the automatically generated reset network of AXI interconnect **ps_8_axi_periph** .

Disconnect input **S00_ARESETN** of **ps_8_axi_periph** from the network driven by output **peripherial_aresetn[0:0]** of **proc_sys_reset_4** block.

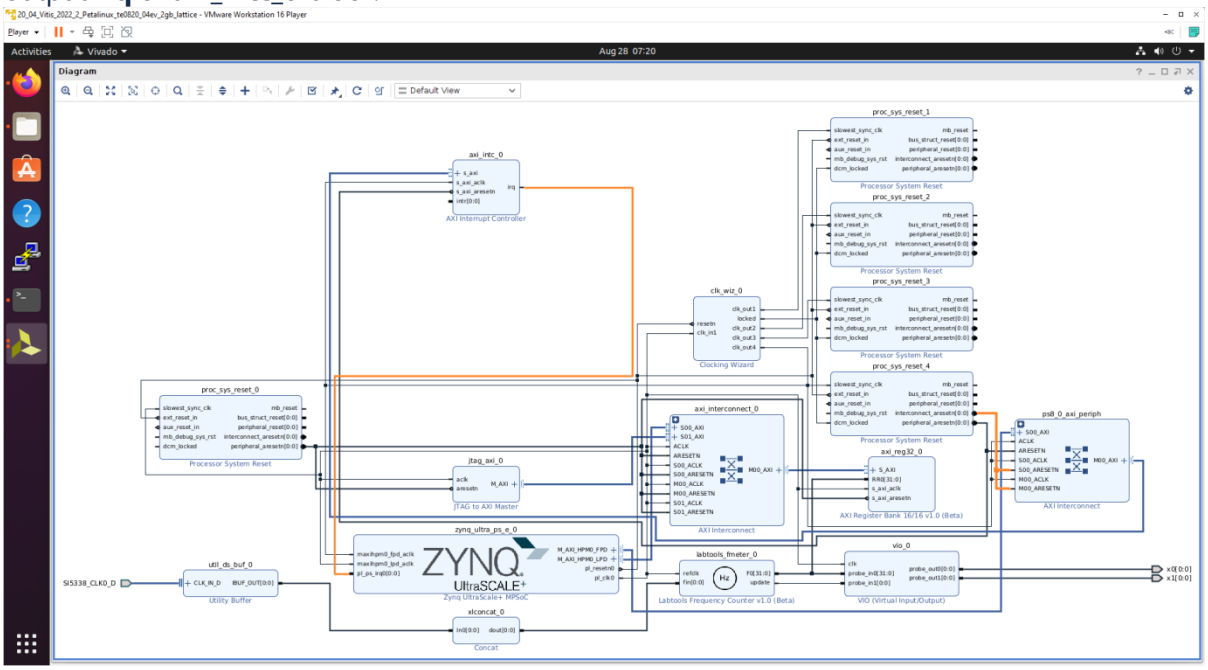
Connect input **S00_ARESETN** of **ps_8_axi_periph** block with output **interconnect_aresetn[0:0]** of **proc_sys_reset_4** block.

Disconnect input **M00_ARESETN** of **ps_8_axi_periph** block from the network driven by output **peripherial_aresetn[0:0]** of **proc_sys_reset_4** block.

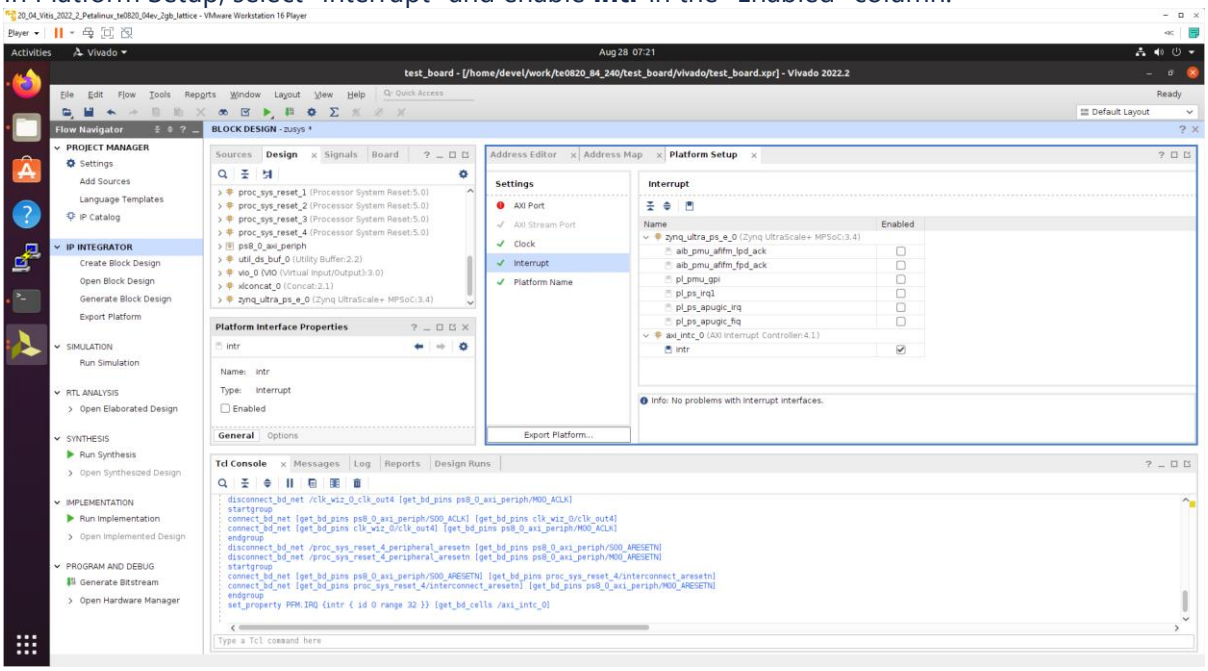
Connect input **M00_ARESETN** of **ps_8_axi_periph** to output **interconnect_aresetn[0:0]** of **proc_sys_reset_4** block.

This modification will make the reset structure of the AXI interconnect **ps_8_axi_periph** block identical to the future extensions of this interconnect generated by the Vitis extensible design flow.

Connect the interrupt **input pl_ps_irq0[0:0]** of **zynq_ultra_ps_e_0** block with output **irq** of **axi_intc_0** block.



In Platform Setup, select “Interrupt” and enable **intr** in the “Enabled” column.



Rename automatically generated name **ps8_0_axi_periph** of the interconnect to new name: **axi_interconnect_1** . This new name will be used in Platform Setup selection of AXI ports for the extensible platform.

In Platform Setup, select AXI Ports for **zynq_ultra_ps_e_0**:

Select **M_AXI_HPM1_FPD** in column “Enabled”.

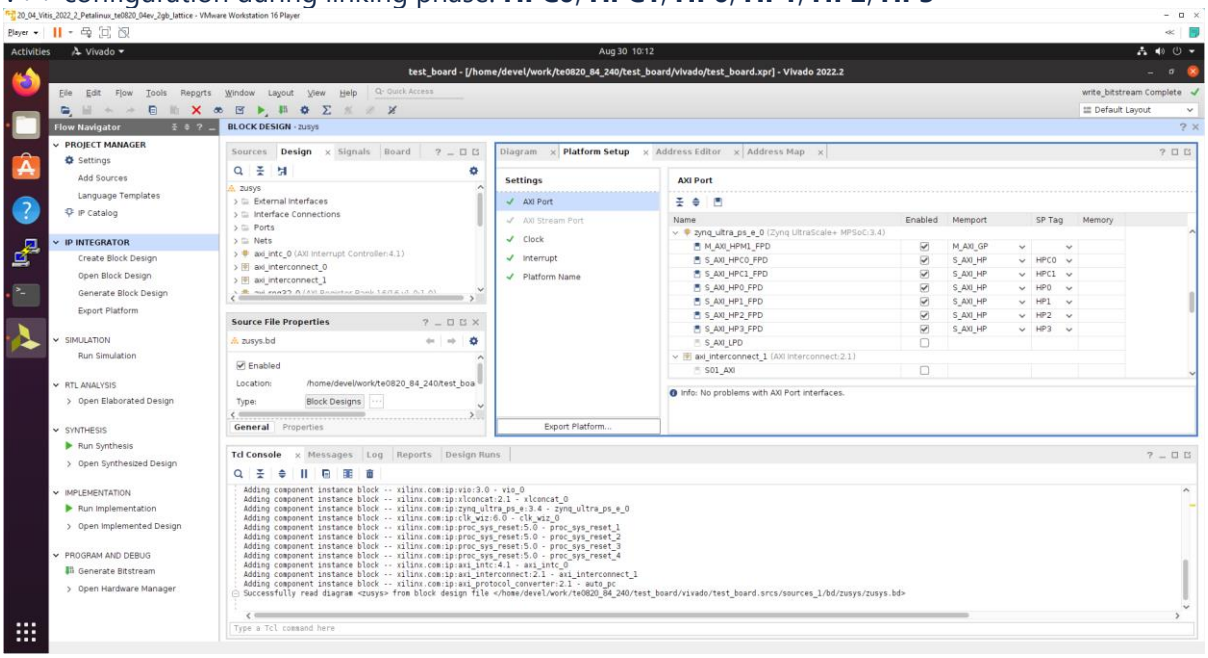
Select **S_AXI_HPC0_FPD** and **S_AXI_HPC1_FPD** in column “Enabled”.

For **S_AXI_HPC0_FPD**, change S_AXI_HPC to **S_AXI_HP** in column “Memport”.

For **S_AXI_HPC1_FPD**, change S_AXI_HPC to **S_AXI_HP** in column “Memport”.

Select **S_AXI_HP0_FPD, S_AXI_HP1_FPD, S_AXI_HP2_FPD, S_AXI_HP3_FPD** in column “Enabled”.

Type into the “sptag” column the names for these 6 interfaces so that they can be selected by v++ configuration during linking phase. **HPC0**, **HPC1**, **HP0**, **HP1**, **HP2**, **HP3**

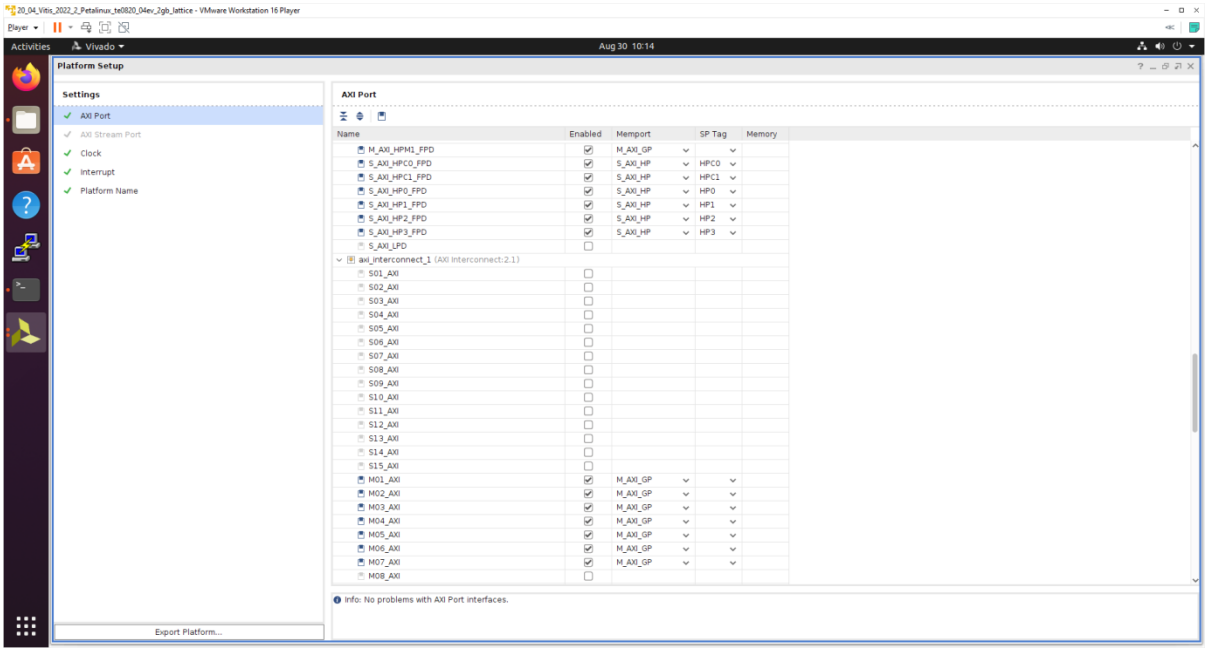


In “Platform Setup”, select AXI Ports for the recently renamed **axi_interconnect_1**:

Select **M01_AXI, M02_AXI, M03_AXI, M04_AXI, M05_AXI, M06_AXI** and **M07_AXI** in column “Enabled”.

Make sure, that you are selecting these AXI ports for the 240 MHz AXI interconnect **axi_interconnect_1**

Keep all AXI ports of the 100 MHz interconnect axi_interconnect_0 unselected. The AXI interconnect axi_interconnect_0 connects other logic and IPs which are part of the initial design.



The modifications of the default design for the extensible platform are completed, now.

In Vivado, save block design by clicking on icon "**Save Block Design**".

Continue the design path with Validate Design.

To continue the manual design path, go to section 3.3 Validate design.

3.2 Fast Track for Creation of Extensible platform HW

HW modifications can be made by sourcing this script in Vivado with open diagram in IP Integrator.

Copy file from the accompanying support package

```
te0820_AI_3_0_eval_package\vivado\script_te0820.txt
```

to

```
~/work/te0820_84_240/test_board/vivado/script_te0820.txt
```

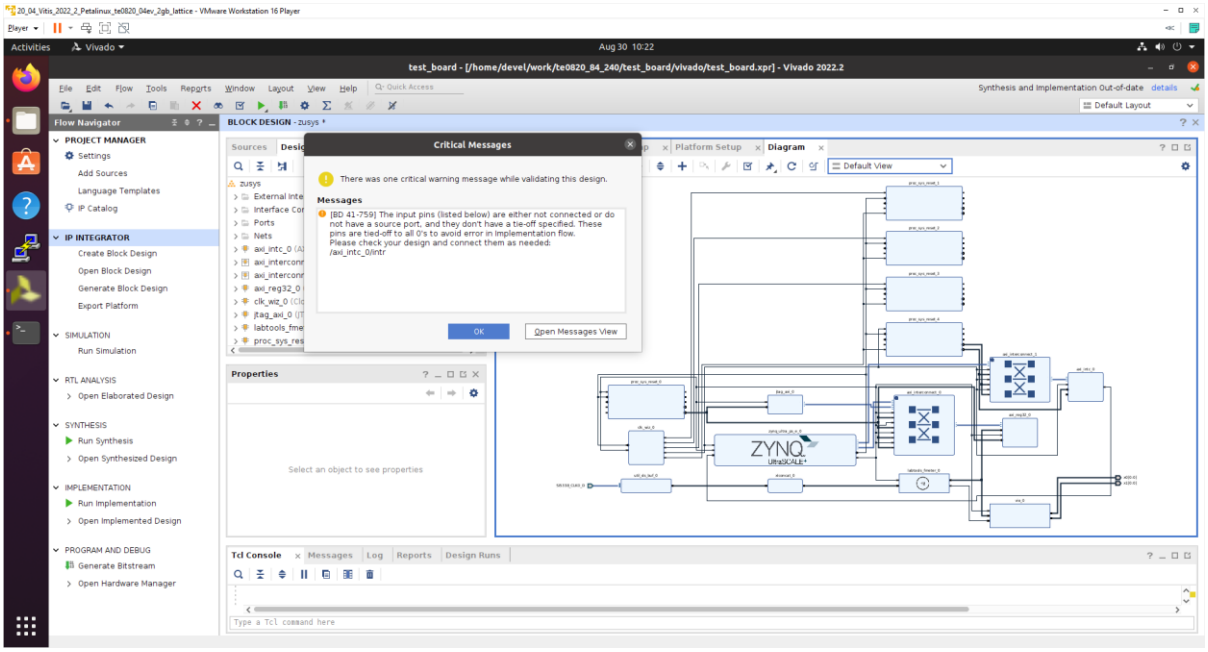
Execute in Vivado Tcl console this command:

```
source script_te0820.txt
```

3.3 Validate Design

Results of HW creation via Manual Track or Fast Track are identical.

Open diagram by clicking on zusys.bd if not already open.
In Diagram window, validate design by clicking on "Validate Design" icon.



Received Critical Messages window indicates that input intr[0:0] of axi_intc_0 is not connected. This is expected. The Vitis extensible design flow will connect this input to interrupt outputs from generated HW IPs.

Click OK.

You can generate pdf of the block diagram by clicking to any place in diagram window and selecting “Save as PDF File”. Use the offered default file name:

```
~/work/te0820_84_240/test_board/vivado/zusys.pdf
```

3.4 Compile Created HW and Custom SW with Trenz Scripts

In Vivado Tcl Console, type following script and execute it by Enter. It will take some time to compile HW. HW design and to export the corresponding standard XSA package with included bitstream.

```
TE::hw_build_design -export_prebuilt
```

An archive for standard non-extensible system is created:

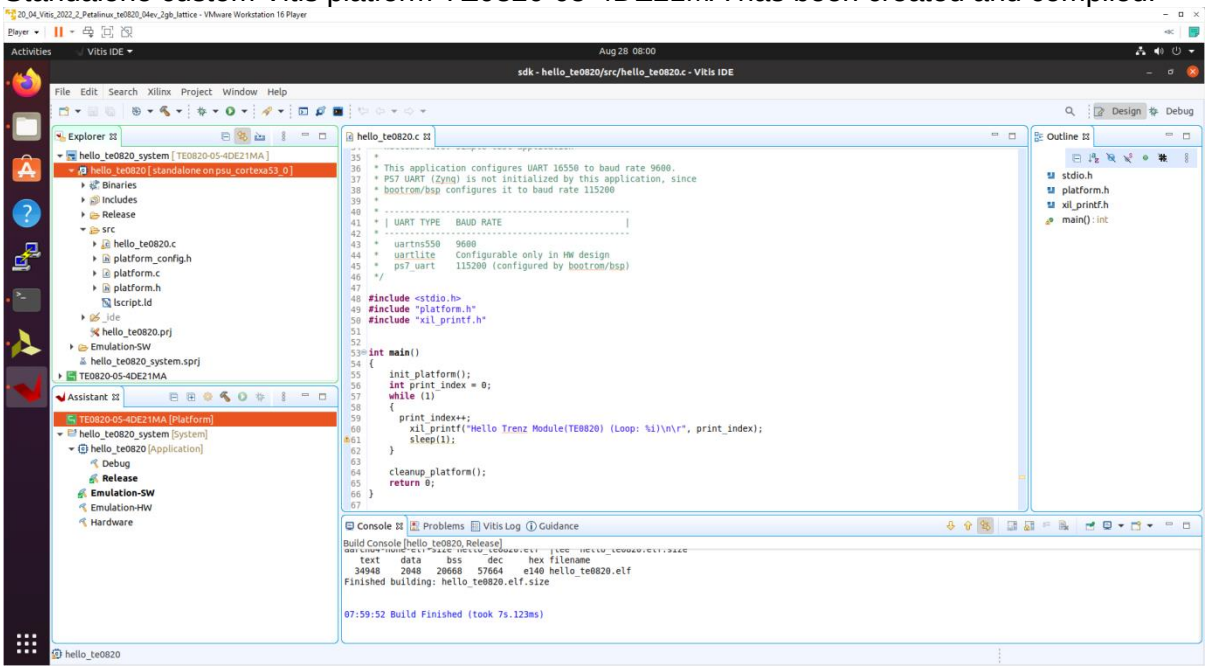
```
~/work/te0820_84_240/test_board/vivado/test_board_4ev_1e_2gb.xsa
```

In Vivado Tcl Console, type the following script and execute it by Enter. It will take some time to compile.

```
TE::sw_run_vitis -all
```

After the script controlling SW compilation is finished, the Vitis SDK GUI is opened.

Close the Vitis “Welcome” page.
Compile the two included SW projects.
Standalone custom Vitis platform TE0820-05-4DE21MA has been created and compiled.



The TE0820-05-4DE21MA Vitis platform includes Trenz Electronic custom first stage boot loader in folder **zynqmp_fsbl**. It includes SW extension specific for the Trenz module initialisation.

This custom zynqmp_fsbl project has been compiled into executable file fsbl.elf. It is located in:

```
~/work/te0820_84_240/test_board/prebuilt/software/4ev_1e_2gb/fsbl.elf
```

This customised first stage boot loader is needed for the Vitis extensible platform.
We have used the standard Trenz scripts to generate it for next use in the extensible platform.

Exit the opened Vitis SDK project.

In Vivado top menu select File->Close Project to close project. Click OK.

In Vivado top menu select File->Exit to close Vivado. Click OK**.**

The exported Vitis Extensible Hardware platform named test_board_4ev_1e_2gb.xsa can be found in the vivado folder.

3.5 Copy Created Custom First Stage Boot Loader

Up to now, test_board directory has been used for all development.

```
~/work/te0820_84_240/test_board
```

Create new folders:

```
~/work/te0820_84_240/test_board_pfm/pfm/boot
~/work/te0820_84_240/test_board_pfm/pfm/sd_dir
```

Copy the recently created custom first stage boot loader executable file from

```
~/work/te0820_84_240/test_board/prebuilt/software/4ev_1e_2gb/fsbl.elf
```

to

```
~/work/te0820_84_240/test_board_pfm/pfm/boot/fsbl.elf
```

4 Building Petalinux for Extensible Design Flow with Vitis AI 3.0 Support

4.1 Vitis AI 3.0 support

Download the Vitis-AI 3.0 repository.
In browser, open page:

https://github.com/Xilinx/Vitis-AI/tree/3.0

Click on green Code button and download Vitis-AI-3.0.zip file.
Unzip

```
Vitis-AI-3.0.zip
```

to directory

```
~/Downloads/Vitis-AI
```

Copy

```
 ~/Downloads/Vitis-AI
```

to

```
~/work/Vitis-AI-3.0
```

The directory

```
 ~/work/Vitis-AI-3.0
```

contains the Vitis-AI 3.0 framework, now.

To install the Vitis-AI 3.0 version of shared libraries into rootfs (when generating system image by PetaLinux) we have to copy recepies `recipes-vitis-ai` to the Petalinux project.

Copy

```
~/work/Vitis-AI-3.0/src/vai_petalinux_recepies/recipes-vitis-ai
```

to

```
~/work/te0802_04_240_vga/test_board/os/petalinux/project-spec/meta-user/
```

Delete file:

```
~/work/te0802_04_240_vga/test_board/os/petalinux/project-spec/meta-user/recipes-vitis-ai/vart/vart_3.0_vivado.bb
```

and keep only the unmodified file:

```
~/work/te0802_04_240_vga/test_board/os/petalinux/project-spec/meta-user/recipes-vitis-ai/vart/vart_3.0.bb
```

File `vart_3.0.bb` will create `vart` libraries for Vitis design flow with dependency on the AMD `xrt` software framework.

4.2 Building Petalinux for Extensible Design Flow

Change directory to the default Trenz Petalinux folder

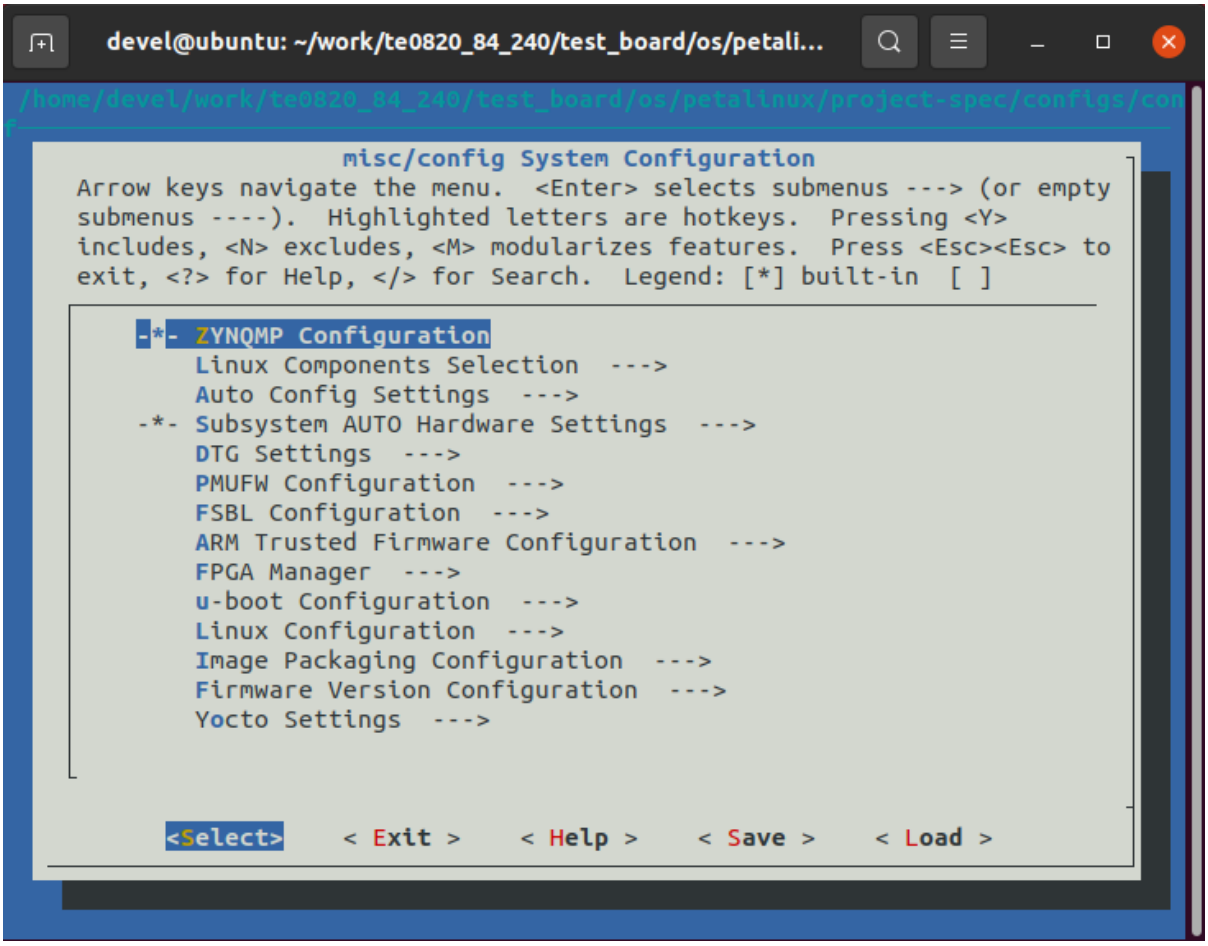
```
~/work/te0820_84_240/test_board/os/petalinux
```

Source Vitis and Petalinux scripts to set environment for access to Vitis and PetaLinux tools.

```
$ source /tools/Xilinx/Vitis/2022.2/settings64.sh

$ source ~/petalinux/2022.2/settings.sh
```

Configure petalinux with the test_board_4ev_2gb.xsa for the extensible design flow by executing:

```
$ petalinux-config --get-hw-description=

~/work/te0820_84_240/test_board/vivado
```



Select **Exit->Yes** to close this window.

In text editor, modify the **user-rootfsconfig** file:

```
~/work/te0820_86_240/test_board/os/petalinux/project-spec/meta-user/conf/user-rootfsconfig
```

In text editor, append these lines:

```
#Note: Mention Each package in individual line
#These packages will get added into rootfs menu entry
CONFIG_startup
CONFIG_webfwu
CONFIG_xrt
CONFIG_xrt-dev
CONFIG_zocl
CONFIG_opencl-clhpp-dev
CONFIG_opencl-headers-dev
CONFIG_packagegroup-petalinux-opencv
CONFIG_packagegroup-petalinux-opencv-dev
CONFIG_dnf
CONFIG_e2fsprogs-resize2fs
CONFIG_parted
CONFIG_resize-part
CONFIG_packagegroup-petalinux-vitisai
CONFIG_packagegroup-petalinux-self-hosted
CONFIG_cmake
CONFIG_packagegroup-petalinux-vitisai-dev
CONFIG_mesa-megadriver
CONFIG_packagegroup-petalinux-x11
CONFIG_packagegroup-petalinux-v4lutils
CONFIG_packagegroup-petalinux-matchbox
CONFIG_packagegroup-petalinux-vitis-acceleration
CONFIG_packagegroup-petalinux-vitis-acceleration-dev
CONFIG_vitis-ai-library
CONFIG_vitis-ai-library-dev
```

```
CONFIG_vitis-ai-library-dbg
```

`xrt, xrt-dev` and `zocl` are required for Vitis acceleration flow.
`dnf` is for package management.
`parted, e2fsprogs-resize2fs` and `resize-part` can be used for ext4 partition resize.

Other included packages serve for natively building Vitis AI applications on target board and for running Vitis-AI demo applications with GUI.

The last three packages will enable use of the Vitis-AI 3.0 recepies for installation of the correspoding Vitis-AI 3.0 libraries into rootfs of PetaLinux.

Launch `rootfs` config:

```
$ petalinux-config -c rootfs
```

All packages will have to have an asterisk `[*]`.

Only `vitis-ai-library-dev` and `vitis-ai-library-dbg` will stay indicated as unselected by: `[ ]`.

Still in the RootFS configuration window, go to root directory by select Exit once.

Enable OpenSSH and Disable Dropbear

Dropbear is the default SSH tool in Vitis Base Embedded Platform. If OpenSSH is used to replace Dropbear, the system could achieve faster data transmission speed over ssh. Created Vitis extensible platform applications may use remote display feature. Using of OpenSSH can improve the display experience.

Go to `Image Features`.
Disable `ssh-server-dropbear` and enable `ssh-server-openssh` and click Exit once.

Go to `Filesystem Packages->misc->packagegroup-core-ssh-dropbear` and disable `packagegroup-core-ssh-dropbear`.

Go to `Filesystem Packages` level by Exit twice.

Go to `console->network->openssh` and enable `openssh, openssh-sftp-server, openssh-sshd, openssh-scp.`

Go to root level by selection of Exit four times.

Enable Package Management

Package management feature can allow the board to install and upgrade software packages on the fly.

In rootfs config go to `Image Features` and enable

`package management` and `debug_tweaks`
options. Click OK, Exit twice and select Yes to save the changes.

4.3 Disable CPU IDLE in Kernel Config

CPU IDLE would cause processors get into IDLE state (WFI) when the processor is not in use. When JTAG is connected, the hardware server on host machine talks to the processor

regularly. If it talks to a processor in IDLE status, the system will hang because of incomplete AXI transactions.

So, it is recommended to disable the CPU IDLE feature during project development phase.

It can be re-enabled after the design has completed to save power in final products.

Launch kernel config:

```
$ petalinux-config -c kernel
```

Ensure the following items are TURNED OFF by entering 'n' in the [ ] menu selection:

`CPU Power Management->CPU Idle->CPU idle PM support`

`CPU Power Management->CPU Frequency scaling->CPU Frequency scaling`

Exit and Yes **to** Save changes**.**

4.4 Add EXT4 rootfs Support

Let PetaLinux generate EXT4 rootfs. In terminal, execute:

```
$ petalinux-config
```

Go to `Image Packaging Configuration`.
Enter into `Root File System Type`

Select `Root File System Type  EXT4`

Change the `Device node` of SD device from the default value
`/dev/mmcblk0p2`

to new value required for the TE0820 module:
`/dev/mmcblk1p2`

Step up to

```
Image Packaging Configuration -->
```

modify `Root filesystem formats` from

```
cpio cpio.gz cpio.gz.u-boot ext4 tar.gz jffs2
```

to

```
ext4
```

Exit and Yes to save changes.

4.5 Let Linux Use EXT4 rootfs During Boot

The setting of which rootfs to use during boot is controlled by bootargs. We would change bootargs settings to allow Linux to boot from EXT4 partition.

In terminal, execute:

```
$ petalinux-config
```

Change **DTG settings->Kernel Bootargs->generate boot args automatically** to NO.

Update **User Set Kernel Bootargs** to:

```
earlycon console=ttyPS0,115200 clk_ignore_unused root=/dev/mmcblk1p2 rw rootwait cma=512M
```

Click **OK**, **Exit** three times and Save.

4.6 Build PetaLinux Image

In terminal, build the PetaLinux project by executing:

```
$ petalinux-build
```

The PetaLinux image files will be generated in the directory:

```
~/work/te0820_84_240/test_board/os/petalinux/images/linux
```

Generation of PetaLinux takes some time and requires Ethernet connection and sufficient free disk space**.**

4.7 Create Petalinux SDK

The SDK is used by Vitis tool to cross compile applications for newly created platfom.

In terminal, execute:

```
$ petalinux-build --sdk
```

The generated sysroot package **sdk.sh** will be located in directory

```
~/work/te0820_84_240/test_board/os/petalinux/images/linux
```

Generation of SDK package takes some time and requires sufficient free disk space**.**
Time needed for these two steps depends also on number of allocated processor cores.

4.8 Copy Files for Extensible Platform

Copy these four files:

Files	From	To
bl31.elf pmufw.elf system.dtb u-boot-dtb.elf	~/work/te0820_84_240/test_board/os/petalinux/images/linux	~/work/te0820_84_240/test_board_pfm/pfm/boot

Rename the copied file `u-boot-dtb.elf` to `u-boot.elf`

The directory

```
~/work/te0820_84_240/test_board_pfm/pfm/boot
```

contains these five files:

```
bl31.elf
fsbl.elf
pmufw.elf
system.dtb
u-boot.elf
```

Copy files:

Files	From	To
boot.scr system.dtb	~/work/te0820_84_240/ test_board/os/petalinux / images/linux	~/work/te0820_84_240/ test_board_pfm/ pfm/sd_dir

Copy file:

File	From	To
init.sh	~/work/te0820_84_240/ test_board/misc/sd	~/work/te0820_84_240/ test_board_pfm/pfm/sd_dir

`init.sh` is an place-holder for user defined bash code to be executed after the boot:

```
#!/bin/sh
normal="\e[39m"
lightred="\e[91m"
lightgreen="\e[92m"
green="\e[32m"
yellow="\e[33m"
cyan="\e[36m"
red="\e[31m"
magenta="\e[95m"

echo -ne $lightred
echo Load SD Init Script
echo -ne $cyan
echo User bash Code can be inserted here and put init.sh on SD
echo -ne $normal
```

4.9 Create Extensible Platform zip File

Create new directory tree:

```
~/work/te0820_84_240_move/test_board/os/petalinux/images
~/work/te0820_84_240_move/test_board/Vivado
~/work/te0820_84_240_move/test_board_pfm/pfm/boot
~/work/te0820_84_240_move/test_board_pfm/pfm/sd_dir
```

Copy all files from the directory:

Files	Source	Destination
all	~/work/te0820_84_240/test_board/os/petalinux/images	~/work/te0820_84_240_move/test_board/os/petalinux/images
all	~/work/te0820_84_240/test_board_pfm/pfm/boot	~/work/te0820_84_240_move/test_board_pfm/pfm/boot
all	~/work/te0820_84_240/test_board_pfm/pfm/sd_dir	~/work/te0820_84_240_move/test_board_pfm/pfm/sd_dir
test_board_4ev_1e_2gb.xsa	~/work/te0820_84_240/test_board/Vivado/test_board_4ev_1e_2gb.xsa	~/work/te0820_84_240_move/test_board/Vivado/test_board_4ev_1e_2gb.xsa

Zip the directory

```
~/work/te0820_84_240_move
```

into ZIP archive:

```
~/work/te0820_84_240_move.zip
```

The archive `te0820_84_240_move.zip` can be used to create extensible platform on the same or on an another PC with installed Ubuntu 20.04 and Vitis tools, with or without installed Petalinux. The archive includes all needed components, including the Xilinx xrt library and the script sdk.sh serving for generation of the sysroot .

The archive has size approximately 3.6 GB and it is valid for the initially selected module number (84). This is the te0820 HW module with xczu4ev-sfvc784-1-e device with 2 GB memory. The extensible Vitis platform will have the default clock 240 MHz.

Move the `te0820_84_240_move.zip` file to an PC disk drive.

Delete:

```
~/work/te0820_84_240_move
~/work/te0820_84_240_move.zip
```

Clean the Ubuntu Trash.

4.10 Generation of SYSROOT

This part of development can be direct continuation of the previous Petalinux configuration and compilation steps.
Alternatively, it is also possible to implement all next steps on an Ubuntu 20.04 without installed PetaLinux Only the Ubuntu 20.04 and Vitis/Vivado installation is needed.
All required files created in the PetaLinux for the specific module (24) are present in the archive: `te0820_84_240_move.zip`
In this case, unzip the archive to the directory:

```
~/work/te0820_84_240_move
```

and copy all content of directories to
`~/work/te0820_84_240`

Delete the **te0820_84_240_move.zip** file and the **~/work/te0820_84_240_move** directory to save filesystem space.

In Ubuntu terminal, change the working directory to:
`~/work/te0820_84_240/test_board/os/petalinux/images/linux`

In Ubuntu terminal, execute script enabling access to Vitis 2022.2 tools.
Execution of script serving for setting up PetaLinux environment is not necessary:

```
$ source /tools/Xilinx/Vitis/2022.2/settings64.sh
```

In Ubuntu terminal, execute script

```
$ ./sdk.sh -d ~/work/te0820_84_240/test_board_pfm
```

SYSROOT directories and files for PC and for Zynq Ultrascale+ will be created in:

```
~/work/te0820_84_240/test_board_pfm/sysroots/x86_64-petalinux-linux
~/work/te0820_84_240/test_board_pfm/sysroots/cortexa72-cortexa53-
xilinx-linux
```

Once created, do not move these sysroot directories (due to some internally created paths).

4.11 Generation of Extensible Platform for Vitis

In Ubuntu terminal, change the working directory to:

```
~/work/te0820_84_240/test_board_pfm
```

Start the Vitis tool by executing

```
$ vitis &
```

In Vitis “Launcher”, set the workspace for the extensible platform compilation:

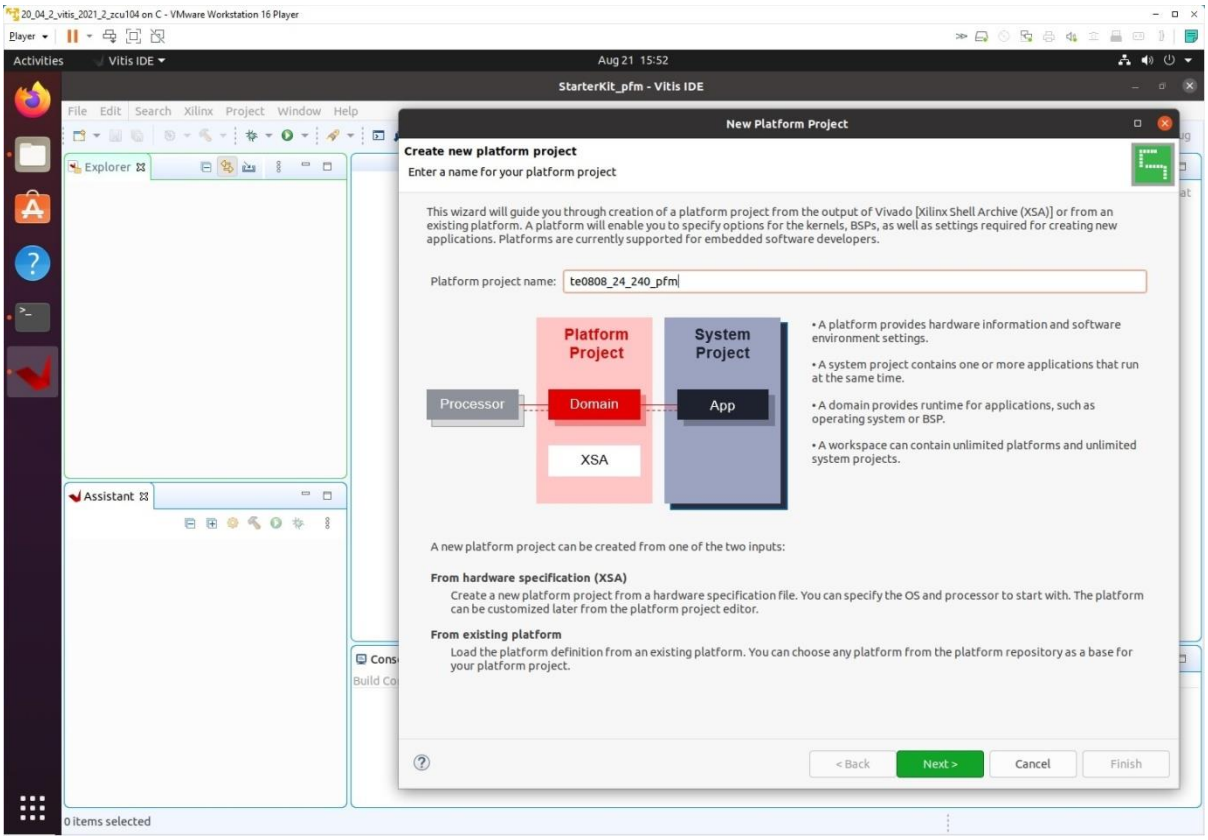
```
~/work/te0820_84_240/test_board_pfm
```

Click on “Launch” to launch Vitis

Close Welcome page.

In Vitis, select in the main menu: `File -> New -> Platform Project`

Type name of the extensible platform: `te0820_84_240_pfm`. Click Next.



Choose for hardware specification for the platform file:

```
~/work/te0820_84_240/test_board/vivado/test_board_4ev_1e_2gb.xsa
```

In “Software specification” select: `linux`
In “Boot Components” unselect `Generate boot components`
(these components have been already generated by Vivado and PetaLinux design flow)

New window `te0820_84_240_pfm` is opened.

Click on `linux on psu_cortex53` to open window Domain: `linux_domain`

In “Description” write: `xrt`

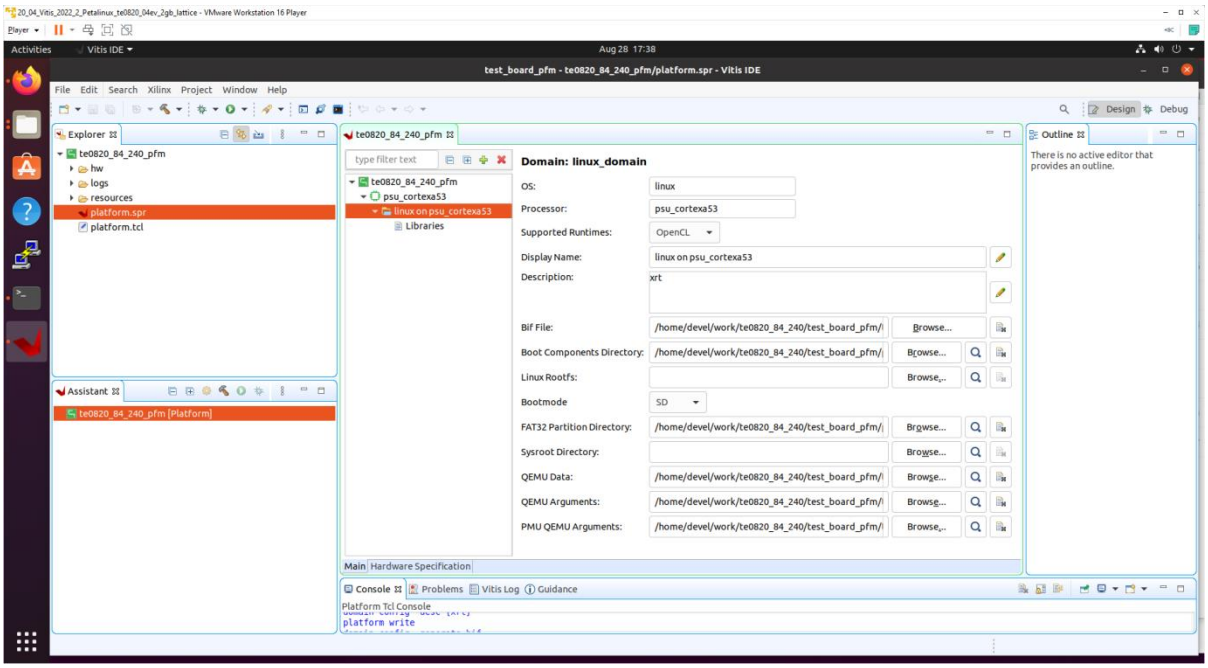
In “Bif File” find and select the pre-defied option: `Generate Bif`

In “Boot Components Directory” select:

```
~/work/te0820_84_240/test_board_pfm/pfm/boot
```

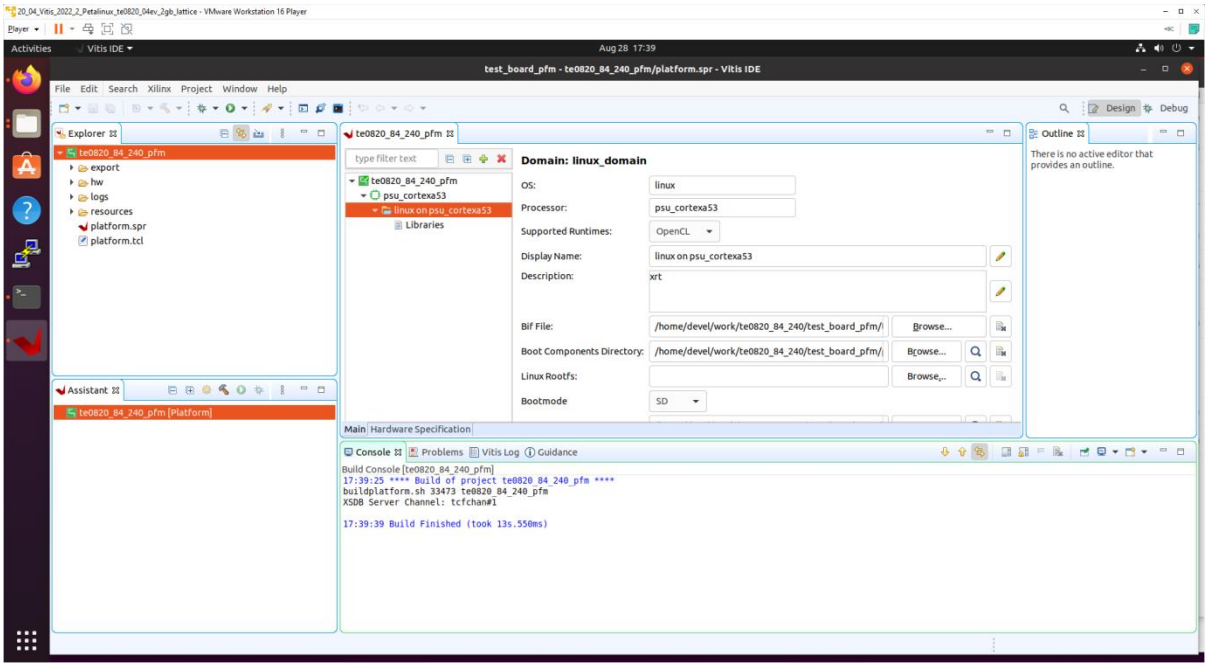
In “FAT32 Partition Directory” select:

```
~/work/te0820_84_240/test_board_pfm/pfm/sd_dir
```



In Vitis IDE “Explorer” section, click on `te0820_84_240_pfm` to highlight it.

Right-click on the highlighted `te0820_84_240_pfm` and select `build project` in the open submenu. Platform is compiled in few seconds.
Close the Vitis tool by selection: `File -> Exit`.



Vits extensible platform `te0820_84_240_pfm` has been created in the directory:

```
~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_240_pfm
```

5 Platform Usage

5.1 Read Platform Info

With Vitis environment setup, platforminfo tool can report XPFM platform information.

```
Platforminfo
~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_
240_pfm/te0820_84_240_pfm.xpfm
```

5.2 Create and Compile Vector Addition Example

Create new directory `test_board_test_vadd` to test Vitis extendable flow example “vector addition”

```
~/work/te0820_84_240/test_board_test_vadd
```

Current directory structure:

```
~/work/te0820_84_240/test_board
~/work/te0820_84_240/test_board_pfm
~/work/te0820_84_240/test_board_test_vadd
```

Change working directory:

```
$cd ~/work/te0820_84_240/test_board_test_vadd
```

In Ubuntu terminal, start Vitis by:

```
$ vitis &
```

In Vitis IDE Launcher, select your working directory

```
~/work/te0820_84_240/test_board_test_vadd
```

Click on `Launch` to launch Vitis.

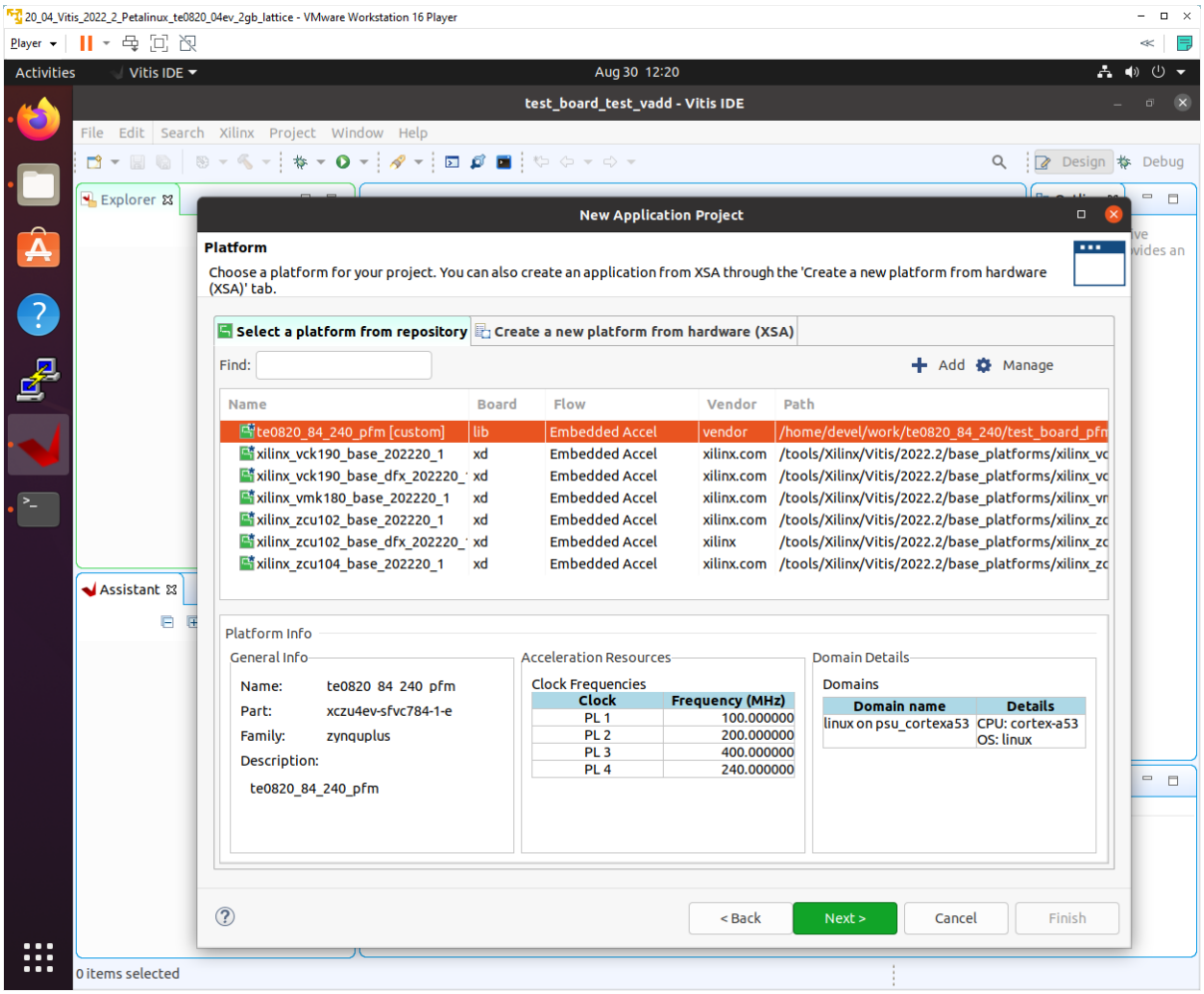
`Select File -> New -> Application project.` Click Next.

Skip welcome page if shown.

Click on `[+ Add]` icon and select the custom extensible platform `te0820_84_240_pfm[custom]` in the directory:

```
~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_
240_pfm
```

We can see available PL clocks and frequencies. PL4 with 240 MHz clock is has been set as default in the platform creation process.



Click Next.
In `Application Project Details` window type into Application project name: `test_vadd`
Click Next.
In `Domain window` type (or select by browse):

Sysroot path:
```
~/work/te0820_84_240/test_board_pfm/sysroots/cortexa72-cortexa53-xilinx-linux
```

Root FS:
```
~/work/te0820_84_240/test_board/os/petalinux/images/linux/rootfs.ext4
```

Kernel Image:
```
~/work/te0820_84_240/test_board/os/petalinux/images/linux/Image
```

Click Next.

In `Templates window`, if not done before, update `Vitis IDE Examples` and `Vitis IDE Libraries`.

Select Host Examples:
In `Find`, type: `vector add` to search for the `Vector Addition` example.

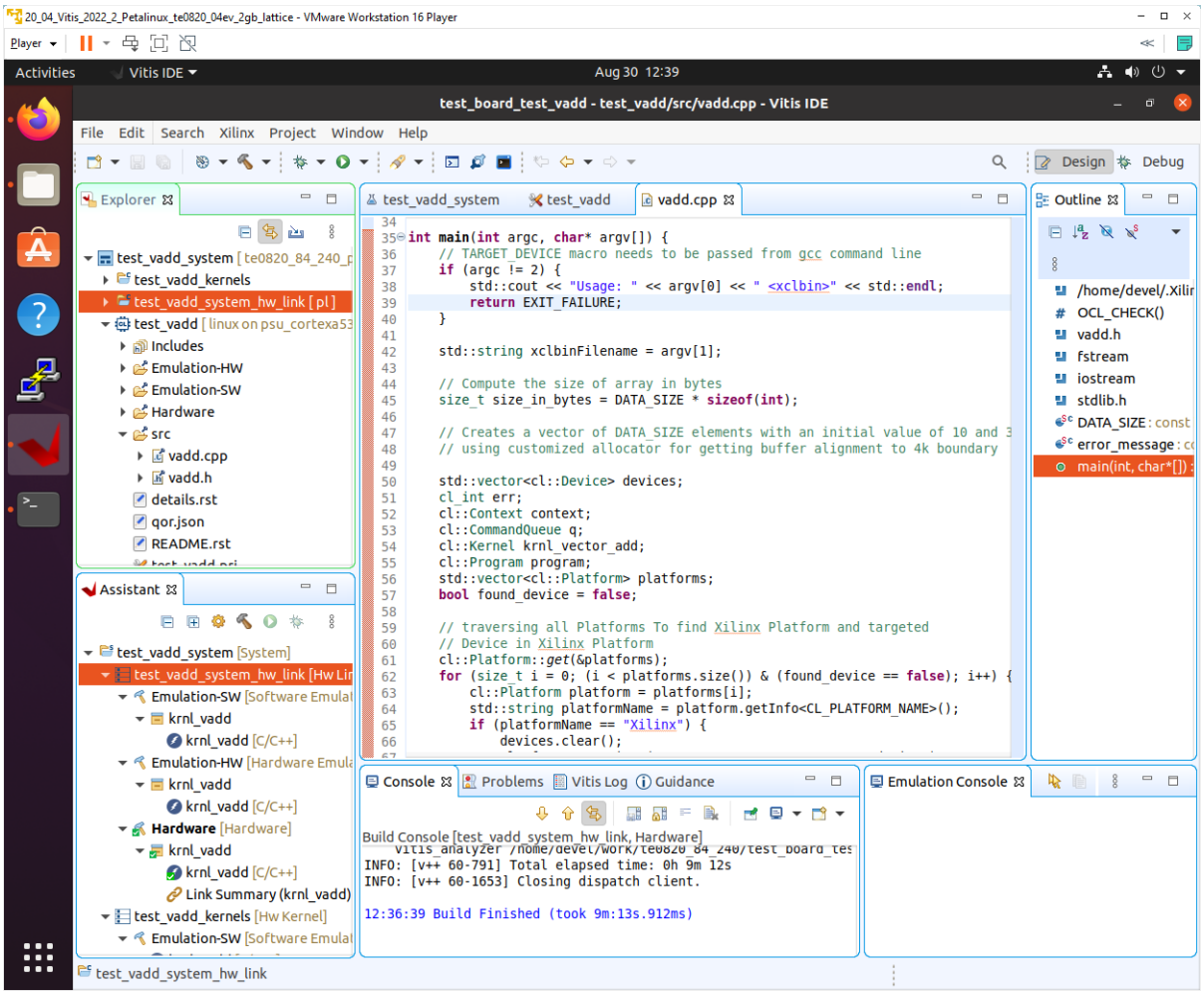
Select: `Vector Addition`
Click Finish
New project template is created.

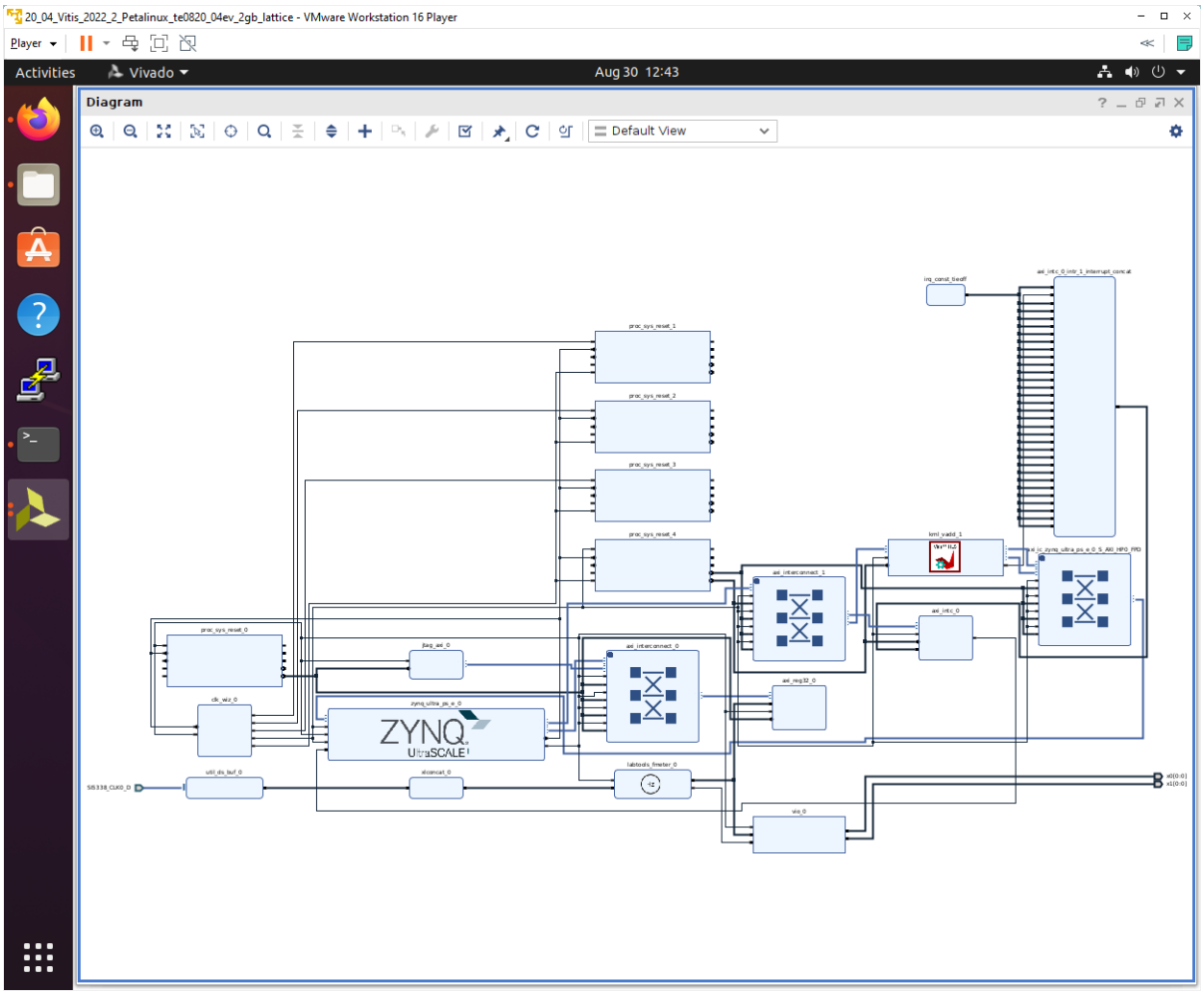
In test_vadd window menu “Active build configuration” switch from `SW Emulation` to `Hardware`.

In “Explorer” section of Vitis IDE, click on: `test_vadd_system[te0820_84_240_pfm]` to select it.

Right Click on: `test_vadd_system[te0820_84_240_pfm]` and select in the opened sub-menu: `Build project`

Vitis will compile. This step can take some time.





Created extended HW with integrated vadd IP block can be open and analysed in Vivado 2022.2.

5.3 Run Compiled test_vadd Example Application

The `sd_card.img` file is output of the compilation and packing by Vitis. It is located in directory:

```
~/work/te0820_84_240/test_board_test_vadd/test_vadd_system/Hardware/package/sd_card.img
```

Write the sd card image `sd_card.img` to SD card.

In Windows Pro 10 (or Windows 11 Pro) PC, inst all program `Win32DiskImager` for this task. Win32 Disk Imager can write raw disk image to removable devices. https://win32diskimager.org/

Insert the SD card to the TE0701-06 carrier board.

Connect PC USB terminal (115200 bps) card to the TE0701-06 carrier board.

Connect Ethernet cable to the TE0701-06 carrier board.

Power on the TE0701-06 carrier board.

In PC, find the assigned serial line COM port number for the USB terminal. In case of Win 10 use device manager.

In PC, open serial line terminal with the assigned COM port number. Speed 115200 bps.

On TE0701-06, reset button to start the system. USB terminal starts to display booting information.

In PC terminal, type:

```
sh-5.0# cd /media/sd-mmcblk1p1/

sh-5.0# ./test_vadd krnl_vadd.xclbin
```

The application test_vadd should run with this output:

```
INFO: Reading krnl_vadd.xclbin

Loading: 'krnl_vadd.xclbin'

Trying to program device[0]: edge

Device[0]: program successful!

TEST PASSED

sh-5.0#
```

The Vitis application has been compiled to HW and evaluated on custom system with extensible custom `te0820_84_240_pfm` platform.

In PC terminal type:

```
# halt
```

System is halted. Messages relate to halt of the system can be seen on the USB terminal.

The SD card can be safely removed from the TE0701-06 carrier board, now.

The TE0701-06 carrier board can be disconnected from power.

System can be connected to the X11 terminal running on your PC Ubuntu with PuTTY application via Ethernet.

Find Ethernet IP address of your board by **ifconfig** command in PetaLinux terminal.
In PC Ubuntu OS, open `PuTTY` application.
In `PuTTY`, set Ethernet IP of your board.
In `PuTTY`, select `checkbox SSH->X11->Enable X11 forwarding`.

Use PC Ubuntu mouse and keyboard. In `PuTTY`, open PetaLinux terminal and login as: user: `root` pswd: `root`.

In opened PetaLinux terminal, start X11 desktop `x-session-manager` by typing:

```
root@Trenz:~# x-session-manager &
```

Click on X11 icon (A Unicode capable `rxvt`)

Terminal opens as an X11 graphic window. In X11 terminal `rxvt`, use Ubuntu PC keyboard and type:

```
sh-5.0# cd /media/sd-mmcblk1p1/

sh-5.0# ./test_vadd krnl_vadd.xclbin
```

The application test_vadd should run with this output:

```
INFO: Reading krnl_vadd.xclbin

Loading: 'krnl_vadd.xclbin'

Trying to program device[0]: edge

Device[0]: program successful!

TEST PASSED

sh-5.0#
```

The test_board has been running the PetaLinux OS and drives simple version of an X11 GUI on Ubuntu desktop.Application test_vadd has been started from X11 xrvt terminal emulator.

Close the rxvt terminal emulator by click ”x” icon (in the upper right corner) or by typing:

```
sh-5.0# exit
```

In X11, click `Shutdown` icon to safely close PetaLinux running on the test board.

System on the test board is halted. Messages related to halt of the system can be seen on the PC USB terminal.

The SD card can be safely removed from the test_board, now.
Close the PC USB terminal application.
The TE0701-06 carrier board can be disconnected from power, now.

6 Vitis AI 3.0 DPUCZDX8V_VAI_v3.0 Installation

This test implements simple AI 3.0 demo to verify DPU integration to our custom extensible platform. This tutorial follows Xilix Vitis Tutorial for zcu104 with necessary fixes and customizations required for our case.

We have to install correct Vitis project with the DPU instance from this repository:

https://github.com/Xilinx/Vitis-AI/tree/3.0/dpu

Page description contains table with supported targets. Use the line if theis table dedicated to DPUCZDX8G DPU for MPSoC and Kria K26 devices.

It is link for download of the programmable logic based DPU, targeting general purpose CNN inference with full support for the Vitis AI ModelZoo.
Supports either the Vitis or Vivado flows on 16nm Zynq® UltraScale+™ platforms.

Click on the Download link in the column: Reference Design

This will result in download of file:

```
~/Downloads/DPUCZDX8V_VAI_v3.0.tar.gz
```

It contains direktory

```
~/Downloads/DPUCZDX8V_VAI_v3.0
```

Copy this directory to the directory:

```
~/work/DPUCZDX8V_VAI_v3.0
```

It contains HDL code for the DPU and also source files and project files to test the DPU with AI resnet50 inference example.

6.1 Create and Build Vitis Design

Create new directory `test_board_dpu_trd` to test Vitis extendable flow example `dpu trd`

~/work/te0820_84_240/test_board_dpu_trd

Current directory structure:

```
~/work/te0820_84_240/test_board
~/work/te0820_84_240/test_board_pfm
~/work/te0820_84_240/test_board_test_vadd
~/work/te0820_84_240/test_board_dpu_trd
```

Change working directory:

```
$cd ~/work/te0820_84_240/test_board_dpu_trd
```

In Ubuntu terminal, start Vitis by:

```
$ vitis &
```

In Vitis IDE Launcher, select your working directory

```
~/work/te0820_84_240/test_board_dpu_trd
```

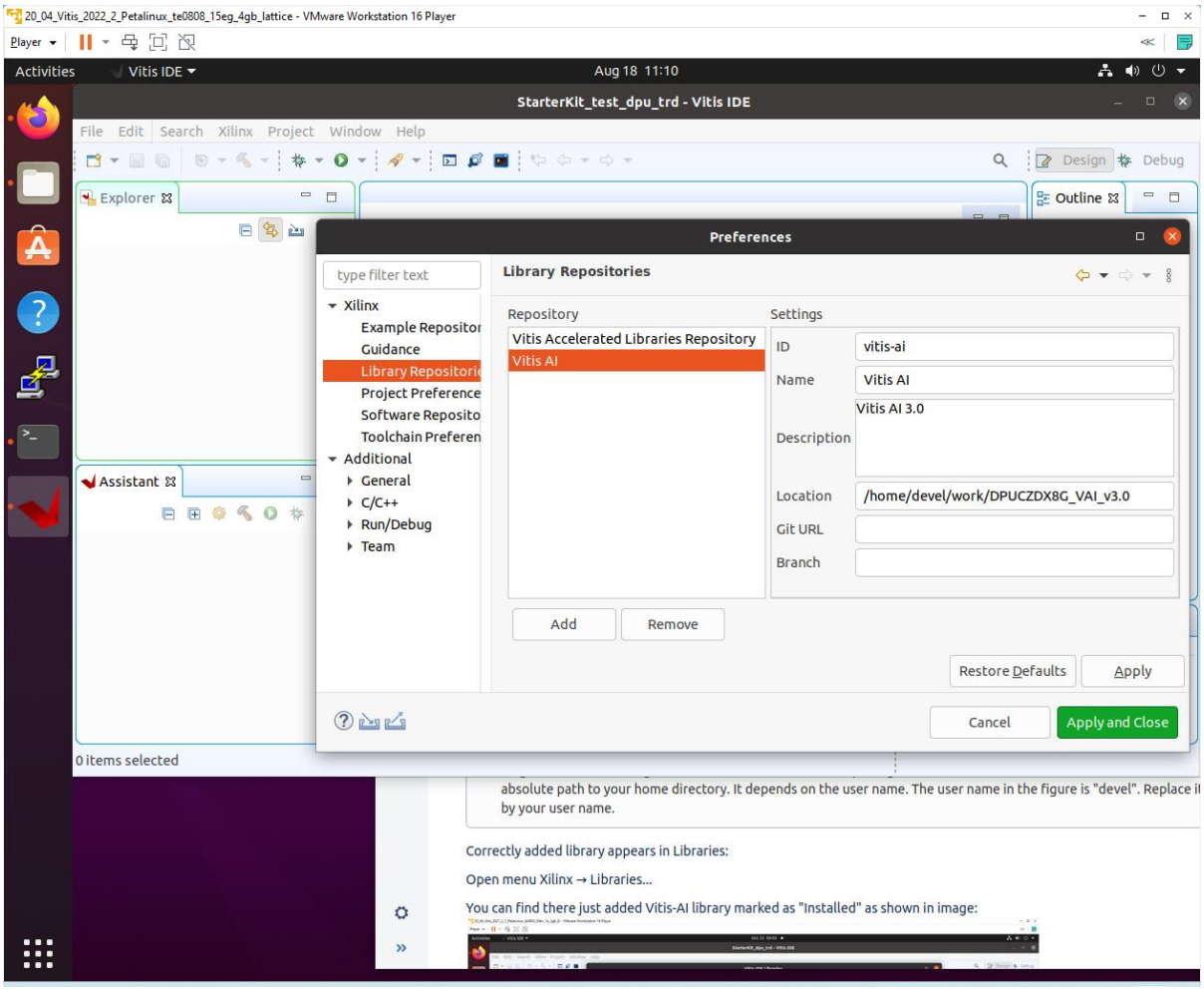
Click on `Launch` to start `Vitis`.

6.2 Add DPU Project template to the Vitis Extensible Flow

Open menu `Window → Preferences`

Go **`to`** `Library Repository` tab

Add `Vitis-AI` by clicking `Add` button and fill the form as shown below, use absolute path to your home folder in field `Location`



Click `Apply` and `Close`.

Field `Location` says that the Vitis-AI repository from github has been allready cloned into

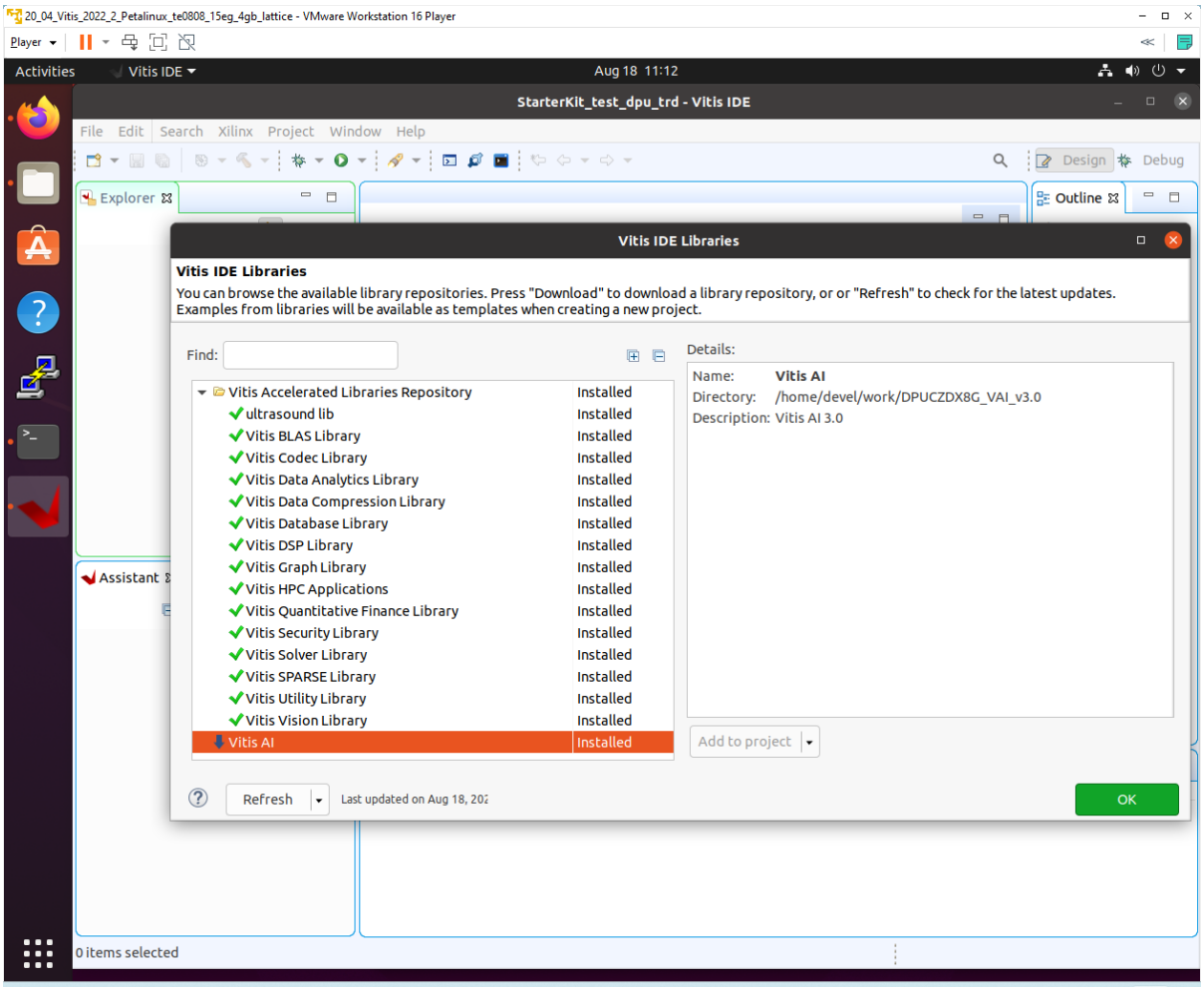
```
~/work/DPUCZDX8V_VAI_v3.0
```

folder, in the stage of Petalinux configuration. Use the `absolute path` to your home directory. It depends on the user name. The user name in the figure is "devel". Replace it by your user name.

Correctly added library appears in Libraries:

Open menu `Xilinx → Libraries...`

You can find there just added Vitis-AI library marked as `Installed`



6.3 Configure Project for the Vitis Extensible Flow with DPU

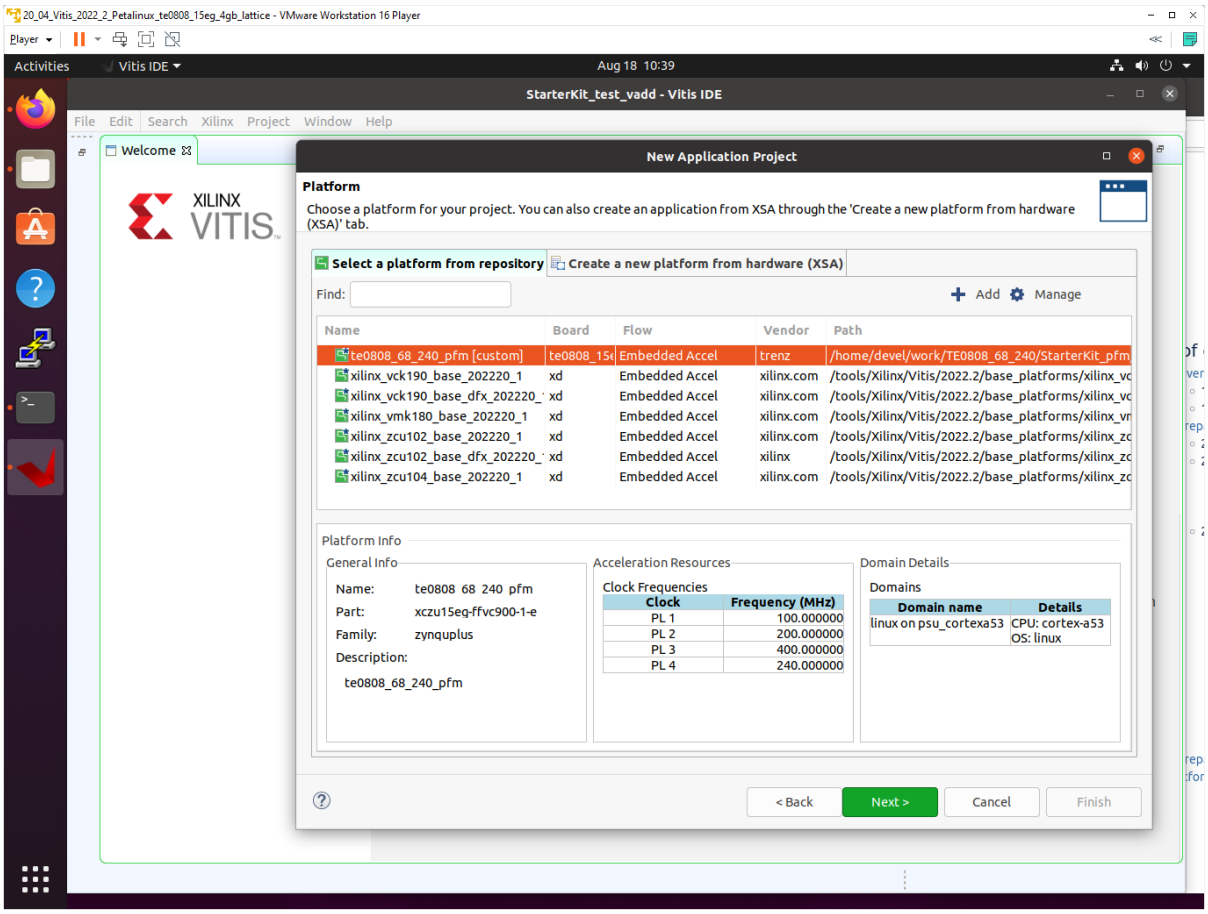
Select `File -> New -> Application project`. Click Next.

Skip welcome page, if it is shown.

Click on `[+ Add]` icon and select the custom extensible platform `te0820_84_240_pfm[custom]` in the directory:

`~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_240_pfm`

We can see available PL clocks and frequencies. PL4 with 240 MHz clock was set as the default in the platform creation process.



Click Next.
In `Application Project Details` window type into Application project name: `dpu_trd`
Click Next.
In `Domain` window type (or select by browse):

"Sysroot path":
```
~/work/te0820_84_240/test_board_pfm/sysroots/cortexa72-cortexa53-xilinx-linux
```

"Root FS":
```
~/work/te0820_84_240/test_board/os/petalinux/images/linux/rootfs.ext4
```

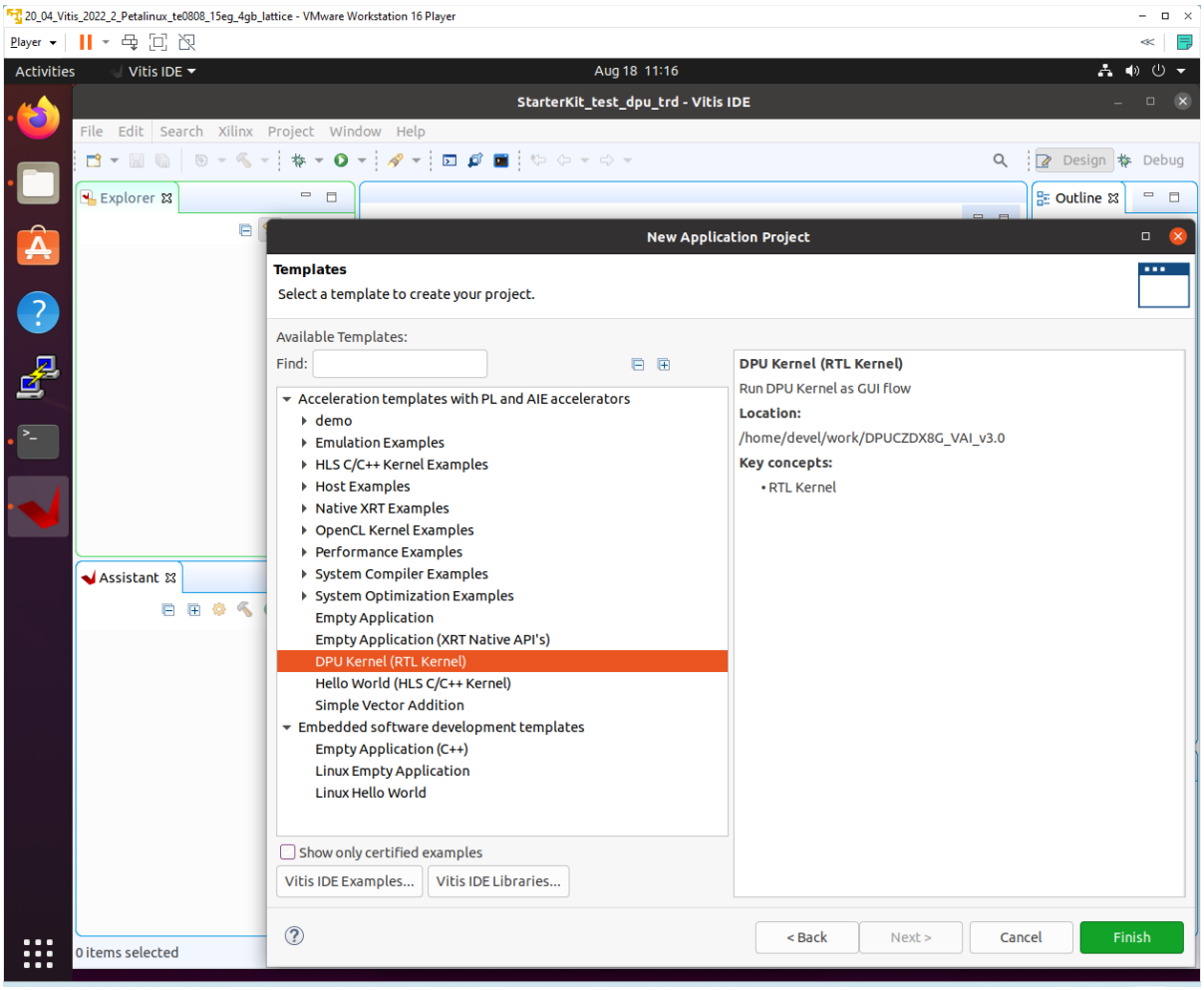
"Kernel Image":
```
~/work/te0820_84_240/test_board/os/petalinux/images/linux/Image
```

Click Next.

In `Templates window`, if not done before, update `Vitis IDE Examples` and `Vitis IDE Libraries`

In "Find", type: `dpu` to search for the `DPU Kernel (RTL Kernel)` example.

Select: `DPU Kernel (RTL Kernel)`



Click Finish
New project template is created.

In dpu_trd window menu `Active build configuration` switch from `SW Emulation` to `Hardware`

File `dpu_conf.vh` located at `dpu_trd_kernels/src/prj/Vitis` directory contains DPU configuration.

Open file `dpu_conf.vh` and change in line 37:

```
`define URAM_DISABLE
```

to

```
`define URAM_ENABLE
```

and save modified file.

In case of module with ID=106 module: TE0820-05-2AE21MA, device xczu2cg-sfvc784-1-e use this new content of file `dpu_conf.vh` to specify DPU with 1024 and use of BRAMs.

```
* Copyright 2019 Xilinx Inc.
*
* Licensed under the Apache License, Version 2.0 (the "License");
```

```
* you may not use this file except in compliance with the License.
* You may obtain a copy of the License at
*
*    http://www.apache.org/licenses/LICENSE-2.0
*
* Unless required by applicable law or agreed to in writing, software
* distributed under the License is distributed on an "AS IS" BASIS,
*  WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or
implied.
* See the License for the specific language governing permissions and
* limitations under the License.
*/

//Setting the arch of DPU, For more details, Please read the PG338



/*====== Architecture Options ======*/
// |-------------------------------------------------------|
// | Support 8 DPU size
// | It relates to model. if change, must update model
// +-------------------------------------------------------+
// | `define B512
// +-------------------------------------------------------+
// | `define B800
// +-------------------------------------------------------+
// | `define B1024
// +-------------------------------------------------------+
// | `define B1152
// +-------------------------------------------------------+
// | `define B1600
// +-------------------------------------------------------+
// | `define B2304
// +-------------------------------------------------------+
// | `define B3136
// +-------------------------------------------------------+
// | `define B4096
```

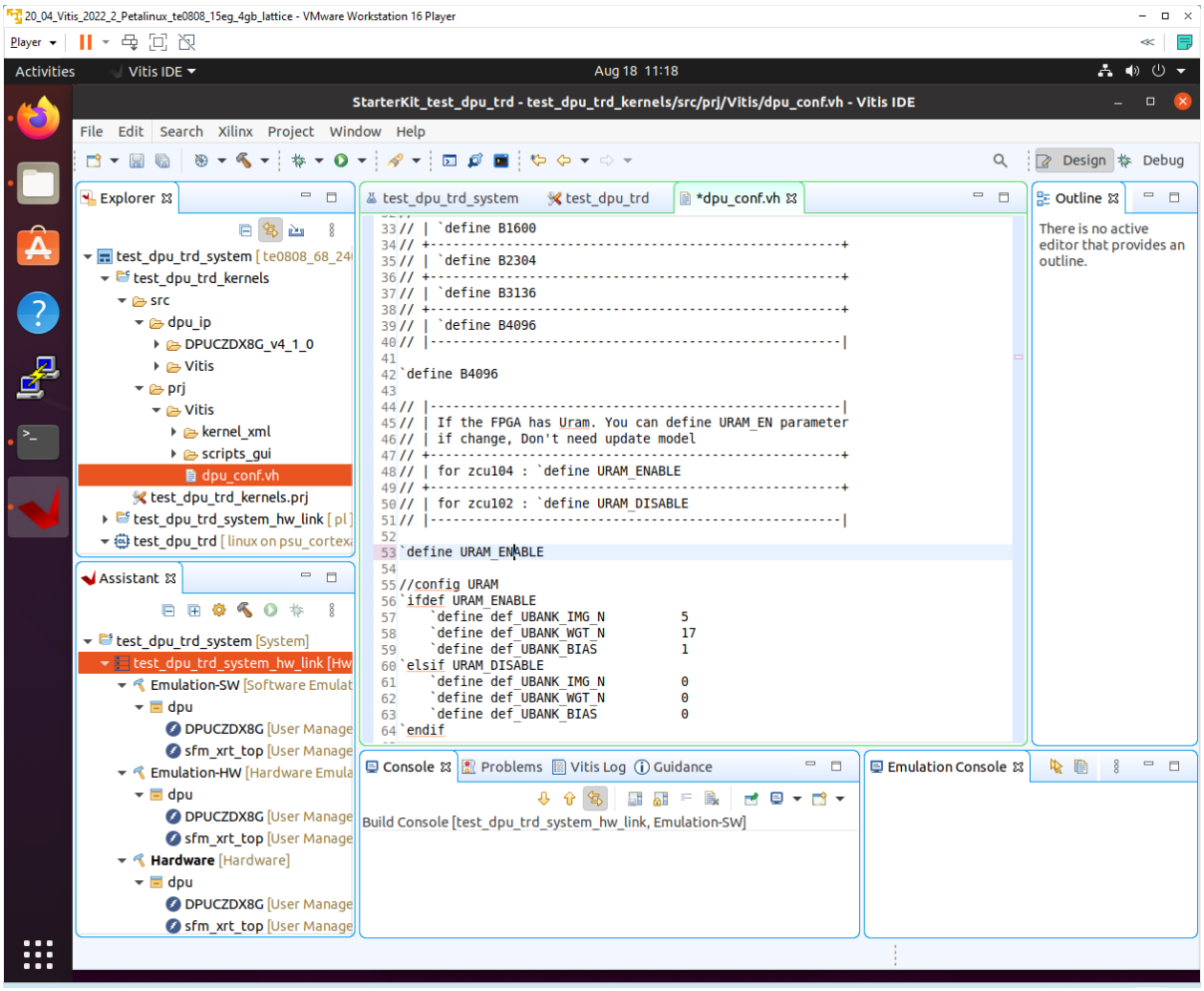
```
// |-----------------------------------------------------|

`define B1024

// |-----------------------------------------------------|
// | If the FPGA has Uram. You can define URAM_EN parameter
// | if change, Don't need update model
// +-----------------------------------------------------+
// | for zcu104 : `define URAM_ENABLE
// +-----------------------------------------------------+
// | for zcu102 : `define URAM_DISABLE
// |-----------------------------------------------------|

`define URAM_DISABLE

//config URAM
`ifdef URAM_ENABLE
    `define def_UBANK_IMG_N          5
    `define def_UBANK_WGT_N          17
    `define def_UBANK_BIAS           1
`elsif URAM_DISABLE
    `define def_UBANK_IMG_N          0
    `define def_UBANK_WGT_N          0
    `define def_UBANK_BIAS           0
`endif

// |-----------------------------------------------------|
// | You can use DRAM if FPGA has extra LUTs
// | if change, Don't need update model
// +-----------------------------------------------------+
// | Enable DRAM  : `define DRAM_ENABLE
// +-----------------------------------------------------+
// | Disable DRAM : `define DRAM_DISABLE
// |-----------------------------------------------------|

`define DRAM_DISABLE
```

```
//config DRAM
`ifdef DRAM_ENABLE
    `define def_DBANK_IMG_N          1
    `define def_DBANK_WGT_N          1
    `define def_DBANK_BIAS           1
`elsif DRAM_DISABLE
    `define def_DBANK_IMG_N          0
    `define def_DBANK_WGT_N          0
    `define def_DBANK_BIAS           0
`endif

// |-----------------------------------------------------|
// | RAM Usage Configuration
// | It relates to model. if change, must update model
// +-----------------------------------------------------+
// | RAM Usage High : `define RAM_USAGE_HIGH
// +-----------------------------------------------------+
// | RAM Usage Low  : `define RAM_USAGE_LOW
// |-----------------------------------------------------|

`define RAM_USAGE_LOW

// |-----------------------------------------------------|
// | Channel Augmentation Configuration
// | It relates to model. if change, must update model
// +-----------------------------------------------------+
// | Enable  : `define CHANNEL_AUGMENTATION_ENABLE
// +-----------------------------------------------------+
// | Disable : `define CHANNEL_AUGMENTATION_DISABLE
// |-----------------------------------------------------|

`define CHANNEL_AUGMENTATION_ENABLE

// |-----------------------------------------------------|
// | ALU parallel Configuration
```

```
// | It relates to model. if change, must update model
// +-----------------------------------------------------+
// | setting 0  : `define ALU_PARALLEL_DEFAULT
// +-----------------------------------------------------+
// | setting 1  : `define ALU_PARALLEL_1
// |-----------------------------------------------------|
// | setting 2  : `define ALU_PARALLEL_2
// |-----------------------------------------------------|
// | setting 3  : `define ALU_PARALLEL_4
// |-----------------------------------------------------|
// | setting 4  : `define ALU_PARALLEL_8
// |-----------------------------------------------------|

`define ALU_PARALLEL_DEFAULT

// +-----------------------------------------------------+
// | CONV RELU Type Configuration
// | It relates to model. if change, must update model
// +-----------------------------------------------------+
// | `define CONV_RELU_RELU6
// +-----------------------------------------------------+
// | `define CONV_RELU_LEAKYRELU_RELU6
// |-----------------------------------------------------|

`define CONV_RELU_LEAKYRELU_RELU6

// +-----------------------------------------------------+
// | ALU RELU Type Configuration
// | It relates to model. if change, must update model
// +-----------------------------------------------------+
// | `define ALU_RELU_RELU6
// +-----------------------------------------------------+
// | `define ALU_RELU_LEAKYRELU_RELU6
// |-----------------------------------------------------|

`define ALU_RELU_RELU6
```

```
// |-----------------------------------------------------|
// | argmax or max Configuration
// | It relates to model. if change, must update model
// +-----------------------------------------------------+
// | enable  : `define SAVE_ARGMAX_ENABLE
// +-----------------------------------------------------+
// | disable : `define SAVE_ARGMAX_DISABLE
// |-----------------------------------------------------|

`define SAVE_ARGMAX_ENABLE

// |-----------------------------------------------------|
// | DSP48 Usage Configuration
// | Use dsp replace of lut in conv operate
// | if change, Don't need update model
// +-----------------------------------------------------+
// | `define DSP48_USAGE_HIGH
// +-----------------------------------------------------+
// | `define DSP48_USAGE_LOW
// |-----------------------------------------------------|

`define DSP48_USAGE_HIGH

// |-----------------------------------------------------|
// | Power Configuration
// | if change, Don't need update model
// +-----------------------------------------------------+
// | `define LOWPOWER_ENABLE
// +-----------------------------------------------------+
// | `define LOWPOWER_DISABLE
// |-----------------------------------------------------|

`define LOWPOWER_DISABLE

// |-----------------------------------------------------|
```

```
// | DEVICE Configuration
// | if change, Don't need update model
// +-----------------------------------------------------+
// | `define MPSOC
// +-----------------------------------------------------+
// | `define ZYNQ7000
// |-----------------------------------------------------|

`define MPSOC
```



This modification is necessary for successful implementation of the DPU on the zcu04-ev module with internal memories implemented in URAMs.

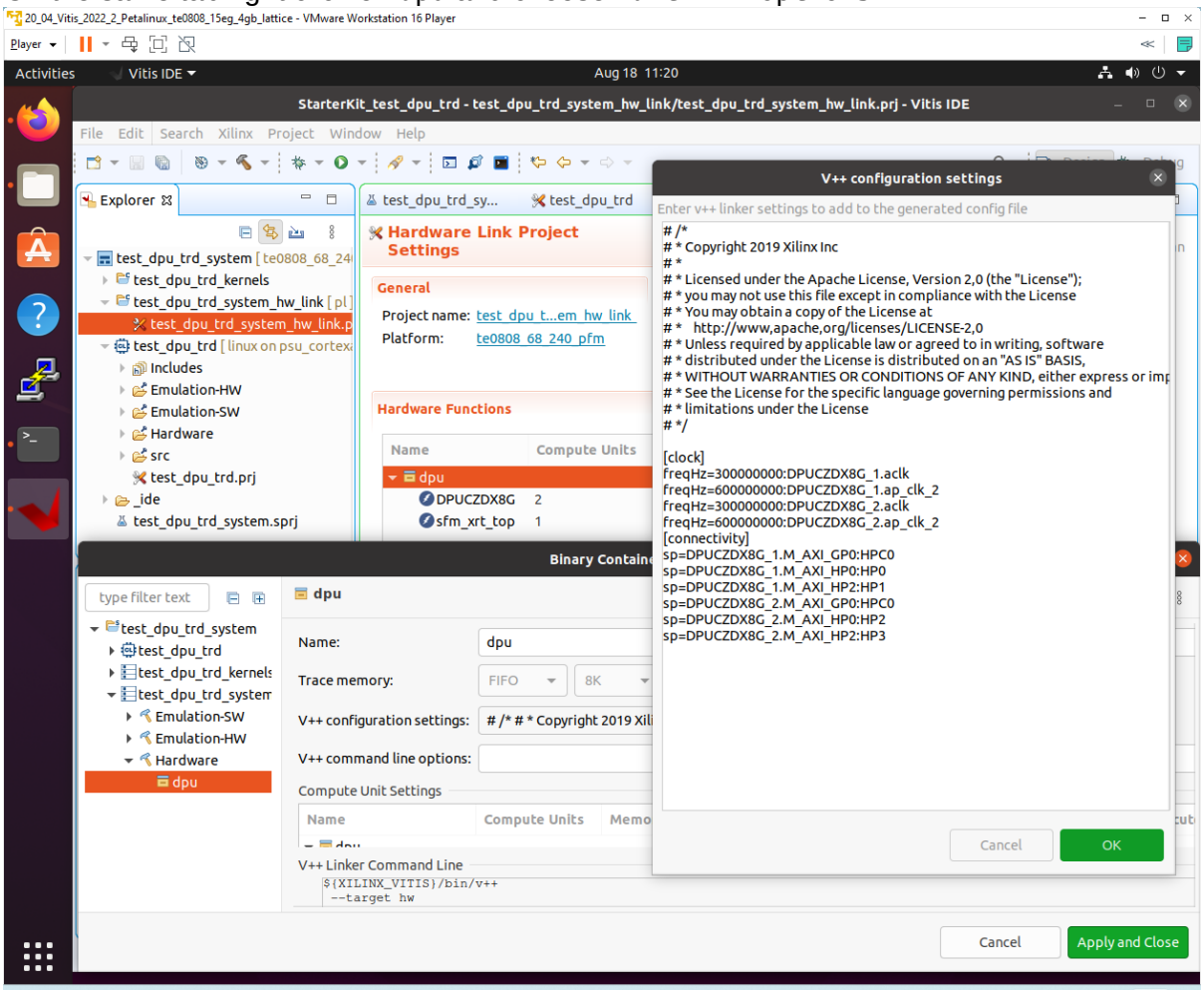
Go to `dpu_trd_system_hw_link` and double click on `dpu_trd_system_hw_link.prj`

Remove `sfm_xrt_top` kernel from binary container by right clicking on it and choosing remove.

Reduce number of DPU kernels to one.

6.4 Configure Connection of DPU kernel

On the same tab right click on dpu and choose `Edit V++ Options`



Click "`...`" button on the line of `V++ Configuration Settings` and modify configuration as follows:

```
[clock]
freqHz=200000000:DPUCZDX8G_1.aclk
freqHz=400000000:DPUCZDX8G_1.ap_clk_2

[connectivity]
sp=DPUCZDX8G_1.M_AXI_GP0:HPC0
sp=DPUCZDX8G_1.M_AXI_HP0:HP0
sp=DPUCZDX8G_1.M_AXI_HP2:HP1
```

6.5 Build the test_dpu_trd Project

In "`Explorer`" section of Vitis IDE, click on:

```
dpu_trd_system[te0802_04_240_vga_pfm]
```

to select it.

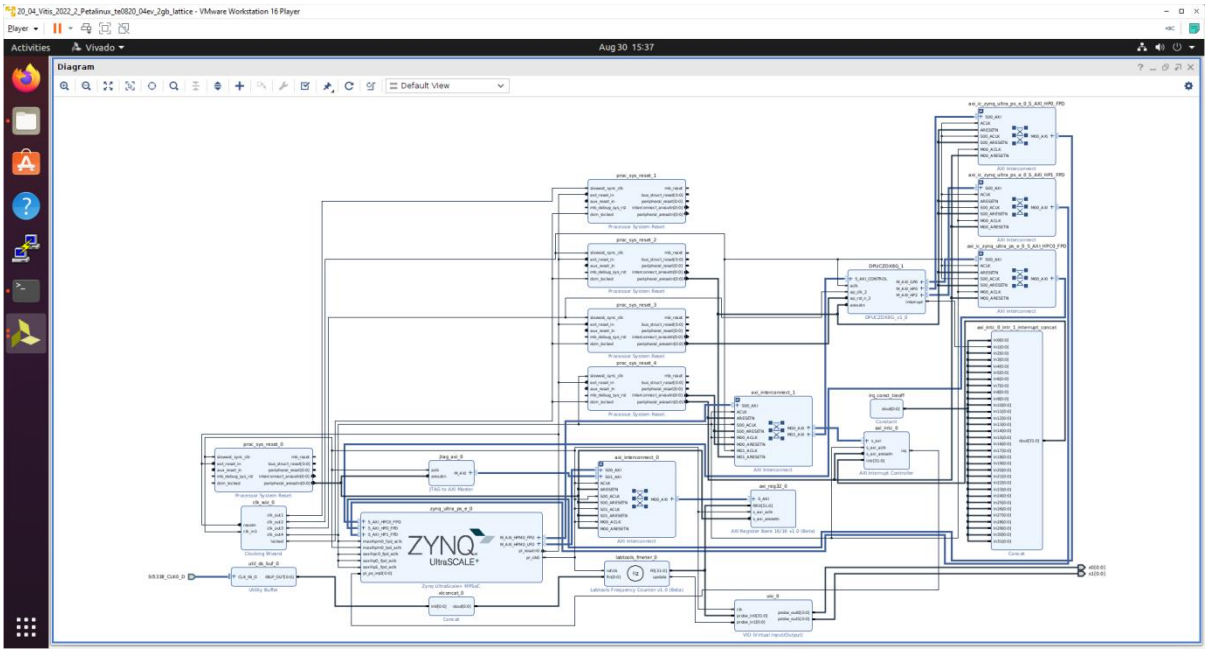
Right Click on:

```
dpu_trd_system[te0802_04_240_vga_pfm]
```

and select in the opened sub-menu: `Build project`

Compilation takes some time (approximately 30 minutes).

Created extended HW with integrated DPU with configuration `B4096` can be open and analysed in Vivado 2022.2



7 Prepare SD card with test_dpu_trd DPU

Write `sd_card.img` to SD card using SD card reader.

The **sd_card.img** file is output of the compilation and packing by Vitis. It is located in directory:

```
~/work/te0820_84_240/test_board_dpu_trd/dpu_trd_system/Hardware/package
```

In Windows 10 (or Windows 11) PC, inst all program **Win32DiskImager** for this task. Win32 Disk Imager can write raw disk image to removable devices.
https://win32diskimager.org/

Boot the board and open terminal on the board either by connecting serial console connection, or by opening ethernet connection to ssh server on the board, or by opening terminal directly using window manager on board. Continue using the embedded board terminal.

Detailed guide how to run embedded board and connect to it can be found in Run Compiled Example Application for Vector Addition.

7.1 Resize EXT4 Partition

Check ext4 partition size by:

```
root@Trenz:~# cd /
root@Trenz:~# df .
Filesystem           1K-blocks      Used Available Use% Mounted on
/dev/root               564048    398340    122364  77% /
```

Resize partition

```
root@Trenz:~# resize-part /dev/mmcblk0p2
```

Check ext4 partition size again, you should see:

```
root@Trenz:~# df . -h
Filesystem                Size      Used Available Use% Mounted on
/dev/root                 6.1G    390.8M      5.4G   7% /
```

The available size would be different according to your SD card size.

Set DISPLAY variable:

```
root@petalinux:~# export DISPLAY=:0.0
```

Set path to Xilinx Firmware:

```
root@petalinux:~# export
XLNX_VART_FIRMWARE=/run/media/mmcblk1p1/dpu.xclbin
```

7.2 Test the Integrated DPUCZDX8G

For both tested modules, the integrated DPU can be tested by command:

```
 xdputil query
```

Command and reply in case of module with ID=84 (DPU configuration B4096):

```
root@trenz:~# xdputil query
{
    "DPU IP Spec":{
        "DPU Core Count":1,
        "IP version":"v4.1.0",
        "generation timestamp":"2023-02-21 21-30-00",
        "git commit id":"7d32c41",
        "git commit time":2023022121,
```

```
        "regmap":"1to1 version"
    },
    "VAI Version":{
        "libvart-runner.so":"Xilinx vart-runner Version: 3.0.0-
c5d2bd43d951c174185d728b8e5bcda3869e0b39  2023-08-27-07:37:08 ",
        "libvitis_ai_library-dpu_task.so":"Xilinx vitis_ai_library
dpu_task Version: 3.0.0-c5d2bd43d951c174185d728b8e5bcda3869e0b39  2023-
01-13 06:58:30 [UTC] ",
        "libxir.so":"Xilinx xir Version: xir-
c5d2bd43d951c174185d728b8e5bcda3869e0b39 2023-08-27-07:36:08",
        "target_factory":"target-factory.3.0.0
c5d2bd43d951c174185d728b8e5bcda3869e0b39"
    },
    "kernels":[
        {
            "DPU Arch":"DPUCZDX8G_ISA1_B4096",
            "DPU Frequency (MHz)":300,
            "IP Type":"DPU",
            "Load Parallel":2,
            "Load augmentation":"enable",
            "Load minus mean":"disable",
            "Save Parallel":2,
            "XRT Frequency (MHz)":300,
            "cu_addr":"0xa0010000",
            "cu_handle":"0xaaab00c1b120",
            "cu_idx":0,
            "cu_mask":1,
            "cu_name":"DPUCZDX8G:DPUCZDX8G_1",
            "device_id":0,
            "fingerprint":"0x101000056010407",
            "name":"DPU Core 0"
        }
    ]
}
root@trenz:~#
```


Command and reply in case of module with ID=106 (DPU configuration B1024):

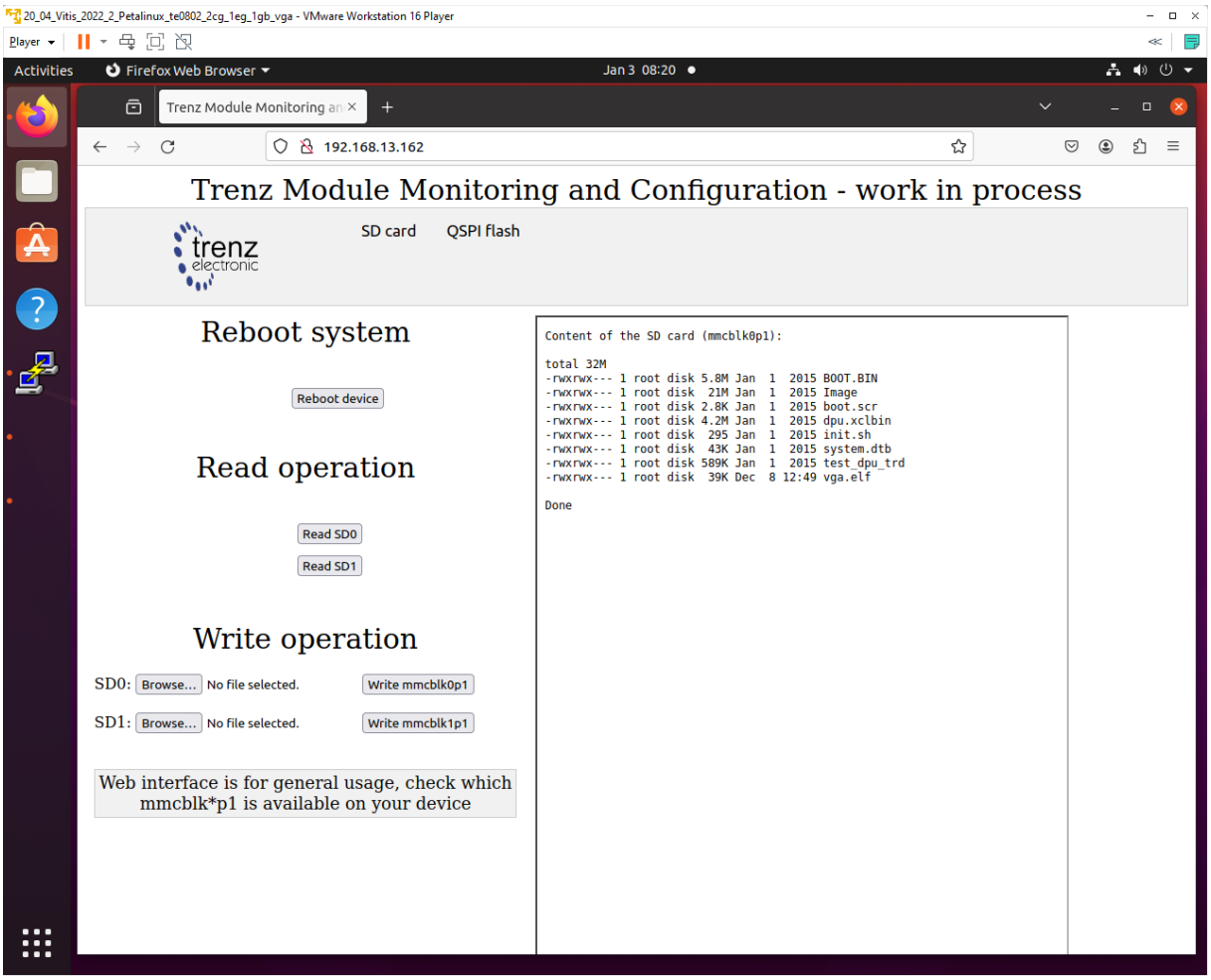
```
root@trenz:~# xdputil query
{
    "DPU IP Spec":{
        "DPU Core Count":1,
        "IP version":"v4.1.0",
        "generation timestamp":"2023-02-21 21-30-00",
        "git commit id":"7d32c41",
        "git commit time":2023022121,
        "regmap":"1to1 version"
    },
    "VAI Version":{
        "libvart-runner.so":"Xilinx vart-runner Version: 3.0.0-
c5d2bd43d951c174185d728b8e5bcda3869e0b39  2024-01-18-07:15:08 ",
        "libvitis_ai_library-dpu_task.so":"Xilinx vitis_ai_library
dpu_task Version: 3.0.0-c5d2bd43d951c174185d728b8e5bcda3869e0b39  2023-
01-13 06:58:30 [UTC] ",
        "libxir.so":"Xilinx xir Version: xir-
c5d2bd43d951c174185d728b8e5bcda3869e0b39 2024-01-18-07:13:09",
        "target_factory":"target-factory.3.0.0
c5d2bd43d951c174185d728b8e5bcda3869e0b39"
    },
    "kernels":[
        {
            "DPU Arch":"DPUCZDX8G_ISA1_B1024",
            "DPU Frequency (MHz)":300,
            "IP Type":"DPU",
            "Load Parallel":2,
            "Load augmentation":"enable",
            "Load minus mean":"disable",
            "Save Parallel":2,
            "XRT Frequency (MHz)":300,
            "cu_addr":"0xa0010000",
            "cu_handle":"0xaaab02346ca0",
            "cu_idx":0,
            "cu_mask":1,
            "cu_name":"DPUCZDX8G:DPUCZDX8G_1",
            "device_id":0,
```

```
            "fingerprint":"0x101000056010402",
            "name":"DPU Core 0"
        }
    ]
}
root@trenz:~#
```

7.3 Remote Monitoring and Configuration Support

The configured OS includes work in progress version of a remote monitoring and configuration support server. It can be used for remote reading of content of the SD card partition mmcblk0p1.

Button Reboot device can be used for system reboot. Ethernet connection is lost, but remote PC www browser remains open and waits for possible reconnection.



After reboot of the evaluation board, the network DHCP server assigns Ethernet address to the evaluation board.

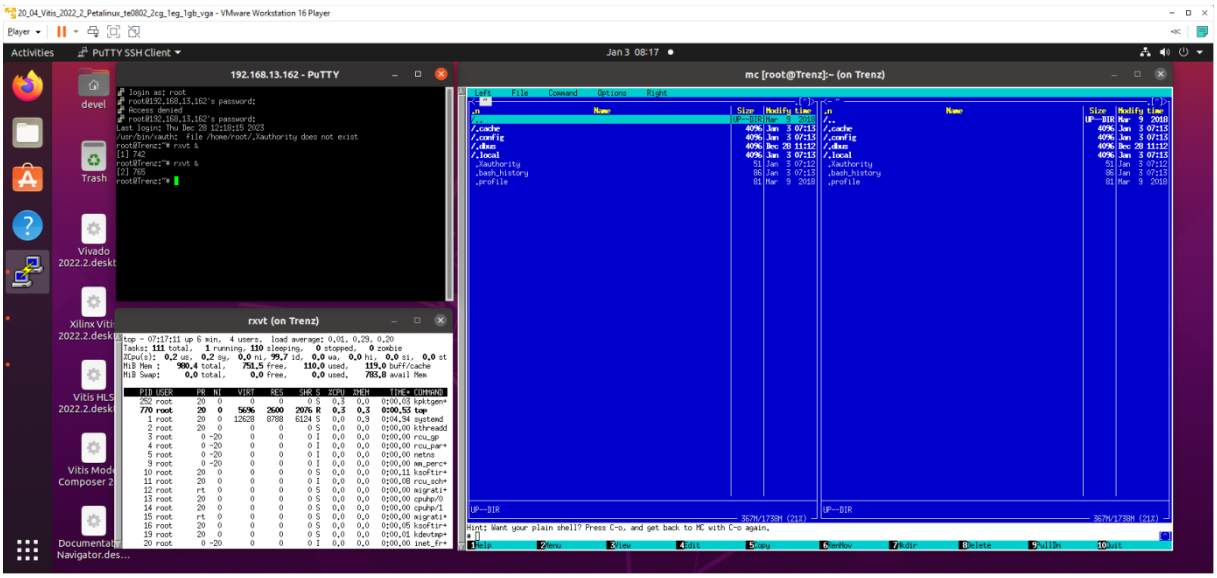
If the network DHCP address assignment algorithm assigns the identical Ethernet address, the page can be refreshed and the connection is re-established again.

If the network DHCP address assignment algorithm assigns different Ethernet address, the connection has to be established on the new Ethernet address.

7.4 Remote Control from Ubuntu X11 Desktop.

The configured OS also supports X11 desktop on remote PC via Ethernet.
In remote PC in Ubuntu OS, in PuTTY terminal utility with ssh Ethernet connection to the board with enabled X11 forwarding.

Openning.
Log in to the evaluation board as user root with pswd root
Start two rxvt terminal emulators by typing in PuTTY terminal:
rxvt &
rxvt &
In first rxvt terminal emulator window start utility
top
In second rxvt terminal emulator start
mc
You can see two applications running on the evaluation board with output on the remote desktop. Remote PC kbd and mouse are used for control of these applications.



Closing.
On remote PC, close top utility by Ctrl-C. Stop mc utility by F10.
Close open terminal emulators by typing exit or by mouse click on x icon in the right top corner of terminal emulator window. Close PuTTY connection by typing exit or by mouse click on x icon in the right top corner of PuTTY window.

7.5 Remote Control in x-session-manager on Ubuntu X11 Desktop.

The configured OS also supports `x-session-manager` on X11 desktop on remote PC connected via Ethernet to the evaluation board.

Opening.
In remote PC in Ubuntu OS, start PuTTY terminal utility with ssh Ethernet connection to the board with enabled X11 forwarding.

Log in to the evaluation board as user root with pswd root
In PuTTY terminal, start `x-session-manager` by typing:

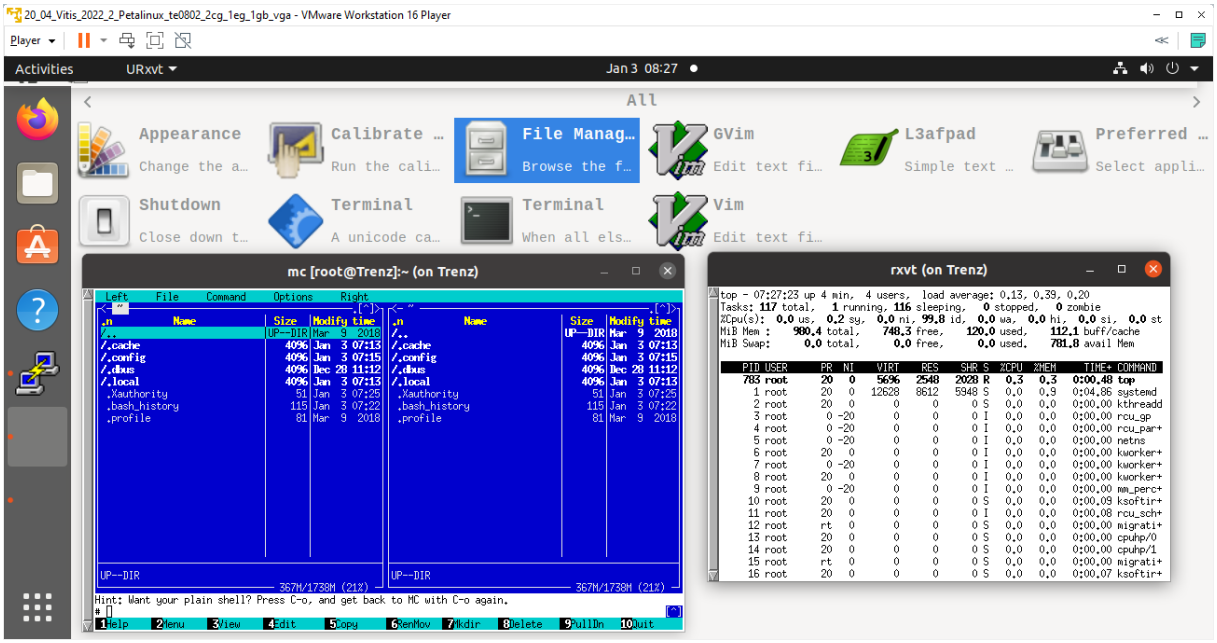
```
x-session-manager &
```

The desktop (displayed on the VGA display of the evaluation board) is also displayed in the remote PC X11 desktop. Start two rxvt terminal emulators by typing in PuTTY terminal:

```
rxvt &

rxvt &
```

In first `rxvt` terminal emulator window start utility `top`
In second `rxvt` terminal emulator start `mc`

You can see two applications running on the evaluation board with output on the remote desktop. Remote PC kbd and mouse are used for control of these applications.



Closing.
On remote PC, close top utility by `Ctrl-C`. Stop `mc` utility by key `F10`.
Close open terminal emulators by typing exit or by mouse click on `x` icon in the right top corner of terminal emulator window. Close `PuTTY` connection by typing exit or by mouse click on `x` icon in the right top corner of `PuTTY` window.

7.6 Display Test Pattern and Test USB Camera

Complete video chain can be tested with output to the X11 desktop.

To display the test pattern, use this gstreamer command:

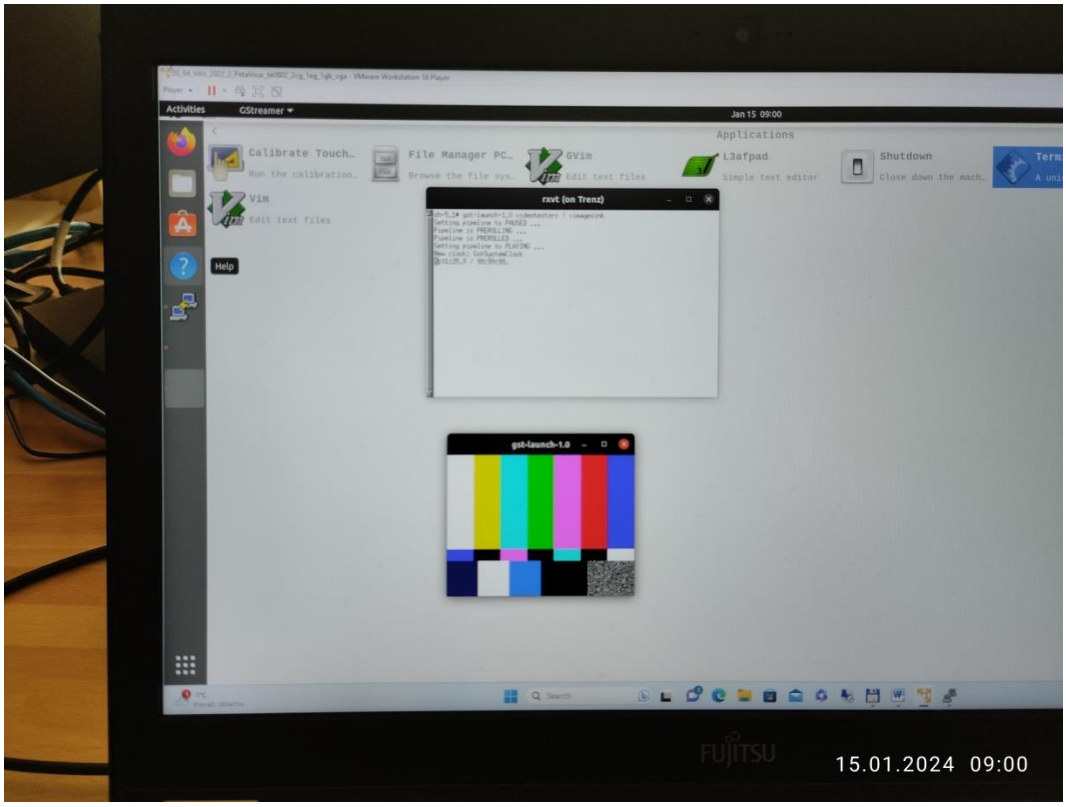
```
gst-launch-1.0 videotestsrc ! ximagesink
```

To display USB camera video, use this gstreamer command:

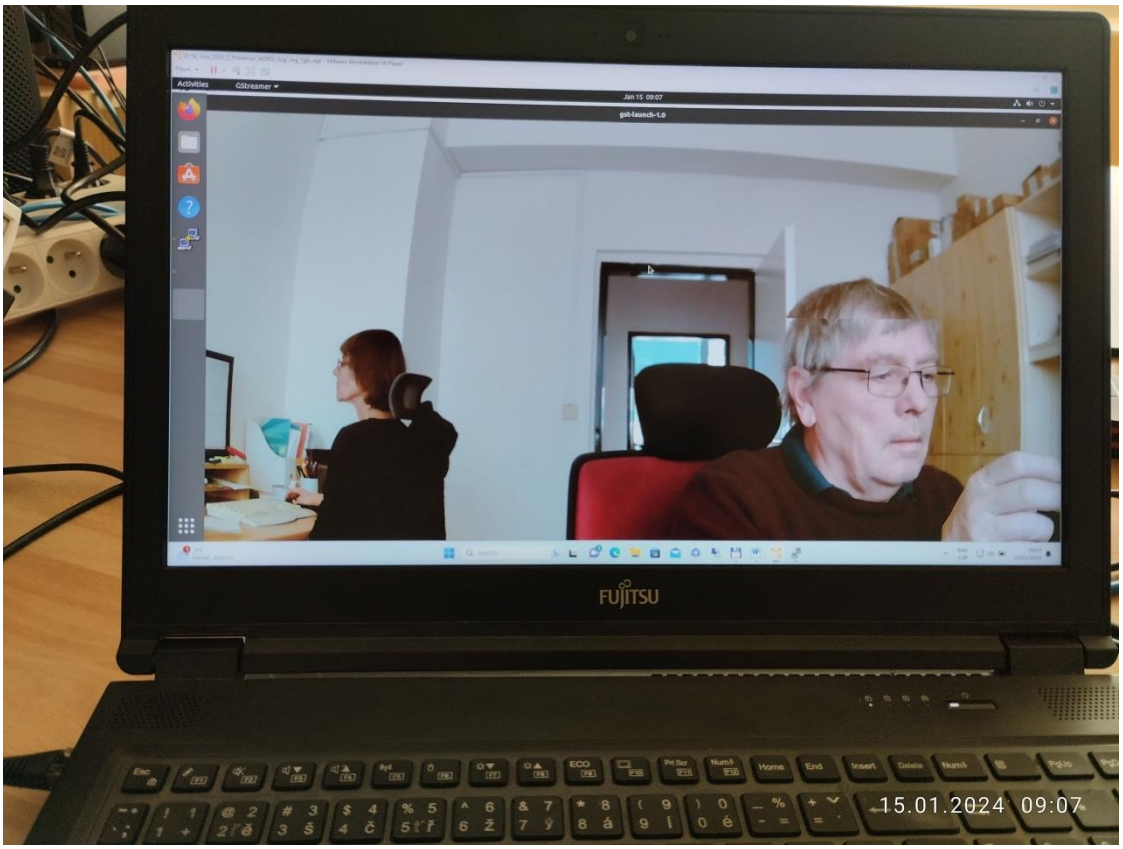
```
gst-launch-1.0 v4l2src device=/dev/video0 ! videoconvert ! ximagesink
```

Video output is directed to the local HD VGA display, if the command is started from local X11 console.

Video output is directed to the remote X11desktop, if the command is started from the remote X11 console.



Test pattern is displayed on remote PC X11 desktop



Full HD video from USB camera is displayed as Full HD on remote PC X11 desktop.

7.7 Vitis AI 3.0 TE-4EV-1E-2GB Module ID=84, TE0701-06, DPU (B4096)

Vitis AI 3.0 exampes	Performance with input from camera e2e [FPS]	Power with camera and VGA [W]	Performance input from file e2e (-t 3) [FPS]	Power with input from file e2e (-t 3) [W]	GigaOps input from file e2e (-t 3) [Gops]
Face detection Model: pt_face-mask-detection_512_512_0.67G_3.0	30.0	10.0	113	9.8	75.7
Vehicle make Model: pt_vehicle-make-classification_VMMR_224_224_3.64G_3.0	30.0	10.5	167	13.6	607.9
Vehicle type Model: pt_vehicle-type-classification_CarBodyStyle_224_224_3.64G_3.0	30.0	10.5	167	13.6	607.9
Vehicle color Model: pt_vehicle-color-classification_VCoR_224_224_3.64G_3.0	30.0	10.5	167	13.6	607.9
General classification Model: pt_resnet50_imagenet_224_224_8.2G_3.0	30.0	11.9	59.6	13.0	488.7
General classification Model: pt_resnet50_imagenet_224_224_0.3_5.8G_3.0	30.0	11.5	69.2	12.7	401.3
General classification Model: pt_resnet50_imagenet_224_224_0.4_4.9G_3.0	30.0	11.2	73.8	12.4	361.6
General classification Model: pt_resnet50_imagenet_224_224_0.5_4.1G_3.0	30.0	11.0	81.1	12.2	332.5
General classification Model: pt_resnet50_imagenet_224_224_0.6_3.3G_3.0	30.0	10.7	91.1	11.9	300.6
General classification Model: pt_resnet50_imagenet_224_224_0.7_2.5G_3.0	30.0	10.6	99.6	11.5	249.0

Measurement conditions:

- TE0820-03-04EV-1EA 2GB module with 12V FAN on TE0701-06 carrier board
- DPU in B4096 configuration
- USB WWW colour camera logi 720p, Logitech, 1280x720p30, 30 FPS
- Remote X11 desktop
- Power supply 12V/5A
- Power measured at the 230V power plug

7.8 Vitis AI 3.0 TE0820-05-2AE21MA module ID=106, TE0707-02, DPU (B1024)

Vitis AI 3.0 exampes	Performance with input from camera e2e [FPS]	Power with camera and VGA [W]	Performance input from file e2e (-t 3) [FPS]	Power with input from file e2e (-t 3) [W]	GigaOps input from file e2e (-t 3) [Gops]
Yolov4 face mask detection Model: pt_face-mask-detection_512_512_0.67G_3.0	20.0	6.6	58.5	6.1	39.2
Vehicleclassification vehicle make Model: pt_vehicle-make-classification_VMMR_224_224_3.64G_3.0	20.0	6.8	43.7	6.7	157.3
Vehicleclassification vehicle type Model: pt_vehicle-type-classification_CarBodyStyle_224_224_3.64G_3.0	20.0	6.8	43.7	6.7	157.3
Classification vehicle color Model: pt_vehicle-color-classification_VCoR_224_224_3.64G_3.0	20.0	6.8	43.7	6.7	157.3
Classification Model: pt_resnet50_imagenet_224_224_8.2G_3.0	18.2	7.5	19.1	6.8	156.6
Classification Model: pt_resnet50_imagenet_224_224_0.3_5.8G_3.0	20.0	7.2	24.8	6.8	143.8
Classification Model: pt_resnet50_imagenet_224_224_0.4_4.9G_3.0	20.0	7.1	28.1	6.8	137.7
Classification Model: pt_resnet50_imagenet_224_224_0.5_4.1G_3.0	20.0	7.0	32.0	6.8	131.2
Classification Model: pt_resnet50_imagenet_224_224_0.6_3.3G_3.0	20.0	6.9	37.3	6.8	123.1
Classification Model: pt_resnet50_imagenet_224_224_0.7_2.5G_3.0	20.0	6.8	44.0	6.8	110.0

Measurement conditions:

- TE0820-05-2AE21MA module (2CG-1E device, 2GB DDR4), TE0707 carrier board
- DPU in B1024 configuration
- USB WWW camera ETERNICO ET201 Full HD, sensor JX_F23, 1920x1080, 20 FPS
- Remote X11 desktop
- Power supply 5V/4A
- Power measured at the 230V power plug

8 References

[1]
Support for STM32H573I-DK web server. (Application note, with evaluation package, UTIA). Not published, yet. To be published for public access from:
https://zs.utia.cas.cz/index.php?ids=projects/eecone
This application and evaluation package will be based on the STM32CubeH5 Firmware Examples for STM32H5xx Series Application based on NetXDuo: **Nx_WebServer.**
This STM application provides an example of Azure RTOS NetX Duo stack usage on STM32H573G-DK board, it shows how to develop Web HTTP server based application.
https://htmlpreview.github.io/?https://raw.githubusercontent.com/STMicroelectronics/STM32CubeH5/master/Projects/STM32CubeProjectsList.html

[2]
Lukáš Kohout, Jiří Kadlec, Zdeněk Pohl: Support for TE0802-02-1BEV2-A board with Vitis AI 3.0 DPU and VGA display (Application note with evaluation package, UTIA). Draft has been provided to partners for review 14.1.2024. **To be published 15.2.2024** for public free access from:
https://zs.utia.cas.cz/index.php?ids=projects/eecone

[3]
Lukáš Kohout, Jiří Kadlec, Zdeněk Pohl: Support for TE0802-02-2AEV2-A board with Vitis AI 3.0 DPU and VGA display (Application note, with evaluation package, UTIA). Draft has been provided to partners for review 14.1.2024. **To be published 15.2.2024** for public access from:
https://zs.utia.cas.cz/index.php?ids=projects/eecone

[4]
Support for module-based systems with TE0821 modules on TE0701 carrier board with Vitis AI 3.0 DPU (Application note, with evaluation package, UTIA). Not published, yet. To be published for free public access from:
https://zs.utia.cas.cz/index.php?ids=projects/eecone

[5]
Support for TE0820 modules with Vitis AI 3.0 DPU (Application note, with evaluation package, UTIA). Not published, yet. To be published for free public access from:
https://zs.utia.cas.cz/index.php?ids=projects/eecone

[6]
Description of compilation of Vitis AI 3.0 models for different configurations of AMD DPUs, (Application note, with evaluation package, UTIA). Not published, yet. To be published for free public access from:
https://zs.utia.cas.cz/index.php?ids=projects/eecone

[7]
TE0802-02-1AEV2-A test board Vitis AI Tutorial
(Vitis 2021.2.1, Vitis AI 2.0, no VGA display support)
https://wiki.trenz-electronic.de/display/PD/TE0802-02-1AEV2-A+test+board+Vitis+AI+Tutorial

[8]
TE0802-02-1AEV2-A test board Vitis AI Tutorial
(Vitis 2021.2.1, Vitis AI 2.0, no VGA display support)
https://wiki.trenz-electronic.de/display/PD/TE0802-02-1AEV2-A+test+board+Vitis+AI+Tutorial

[9]

TE0802-02-1AEV2-A test board Vitis AI Tutorial
(Vitis 2021.2.1, Vitis AI 2.0, no VGA display support)
https://wiki.trenz-electronic.de/display/PD/TE0802-02-1AEV2-A+test+board+Vitis+AI+Tutorial

[10]
MPSoC Development Board with AMD Zynq™ UltraScale+™ ZU2CG and 1 GB LPDDR4, Trenz Electronic.
https://shop.trenz-electronic.de/en/TE0802-02-1BEV2-A-MPSoC-Development-Board-with-AMD-Zynq-UltraScale-ZU2CG-and-1-GB-LPDDR4?c=474

[11]
TE0821 test board Vitis AI Tutorial, v19, prepared by UTIA and published by Trenz Electronics 2.1.2023 (before EECONE start).
https://wiki.trenz-electronic.de/display/PD/TE0821+test+board+Vitis+AI+Tutorial

[12]
TE0821 Resources, TE0821 - 4 x 5 cm SoC module with Xilinx Zynq UltraScale+, prepared and published by Trenz Electronics
https://wiki.trenz-electronic.de/display/PD/TE0821+Resources

[13]
TE0820 test board Vitis AI 3.0 Tutorial, v25, has been prepared by UTIA (before EECONE start) for Trenz Electronics and it has been published by Trenz Electronics 31.8.2023.
https://wiki.trenz-electronic.de/display/PD/TE0820+test+board+Vitis+AI+3.0+Tutorial

[14]
TE0820 - 4 x 5 cm SoC module with AMD Zynq™ UltraScale+™ , prepared and published by Trenz Electronics
https://wiki.trenz-electronic.de/display/PD/TE0820+Resources

[15]
Lukáš Kohout, Zdeněk Pohl and Jiří Kadlec: Xilinx Vitis AI facedetect Demo on Trenz Electronic TE0820 4EV SoM with TE0701 06 Carrier Board and Avnet HDMI In/Out FMC Card; ; (Application note, with evaluation package, UTIA). Published 7.2.2023, (before EECONE start, with acknowledgement to project StorAIge No. 101007321).
https://zs.utia.cas.cz/index.php?ids=results&id=te0820_4ev_vitis_ai_vcu

[16]
Lukáš Kohout, Zdeněk Pohl and Jiří Kadlec: Xilinx Vitis AI facedetect and resnet50 Demo on Trenz Electronic TE0802 02 with ZU2CG and 1 GB LPDD4; Published 16.2.2023, (before EECONE start, with acknowledgement to project StorAIge No. 101007321).
https://zs.utia.cas.cz/index.php?ids=results&id=te0802_2cg_vitis_ai_resnet50

[17]
Zdeněk Pohl, Lukáš Kohout, Jiří Kadlec: Xilinx Vitis AI 'facedetect' and 'resnet50' Demo on Trenz Electronic TE0821-01-2cg-4GB SoM + TE0706-3 Carrier; (Application note, with evaluation package, UTIA). Published 18.1.2023, (before EECONE start, with acknowledgement to project StorAIge No. 101007321).
https://zs.utia.cas.cz/index.php?ids=results&id=te0821_2cg_vitis_ai