

Application Note



Support for TE0820 modules with Vitis AI 3.0 DPU

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Revision history

| Rev. | Date | Author | Description |
|------|-----------|--------|--|
| v01 | 1.2.2024 | J.K | Initial release |
| v02 | 2.2.2024 | J.K | Manual creation of extensible platform |
| v03 | 20.2.2024 | J.K | Added fast track script |
| | | | |

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https://zs.utia.cas.cz/index.php?ids=projects/eecone

https://eecone.com/eecone/home/



https://sp.utia.cas.cz

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1 Introduction

EECONE project <u>https://eecone.com/eecone/home/</u> work package 4, task 4.3 is investigating measures to support second life of electronics due to modular design.

Work package 4 task 4.4 is investigating measures to support extension of life of electronics due to methodology of support used custom platform to adapt for the in-time-evolving design tools and embedded Linux PetaLinux operating system.

UTIA AV CR, v.v.i. (Institute of Information Theory and Automation of the Czech Academy of Sciences, in short UTIA) is not-for profit research institute located in Prague, Czech Republic. UTIA is involved as partner in both tasks, T4.3 and T4.4.

Both EECONE task require specification of comparable reference systems which are based on modular HW with potential for "second life" by reuse of modules or use cost optimized PCB HW without modularity.

Systems (with HW modularity or low cost single PCB) should be capable to perform similar challenging tasks. Systems have to be capable to accelerate in HW AI inference algorithms with video camera input for edge application like person detection, face detection, car-make or car-type detection and graphical output to local display or to the remote PC connected by wired Ethernet in a local network.

Systems should also support remote monitoring and control from remote PC connected by wired Ethernet in a local network.

The investigated measures and methodologies to support "second life" of electronic modules (T4.3) and measures to support extension of life of electronics (T4.4) due to methodology of support used custom platform to adapt for the in-time-evolving design tools and embedded Linux PetaLinux operating system. We target developers designing the final commercial, Al inference based edge applications, mainly in the area of home automation.

Based on these requirements UTIA have selected two types of systems:

- Low cost systems. See [2], [3]
- Modul based systems. See [4] and [5]. [5] is this application note.

Both compared types of systems use STMicroelectronic STM32H573I-DK board for:

- local system control on small graphical touch screen display
- remote system control from www browser based on www-server or secure communication based on mqtt client. Board is supported by STMicroelectronic CubeMX SW framework and also by NetXDuo SW framework on top of ThreadX OS and FileX SW package.

The MCU used on STM32H573I-DK board is a 40nm chip with 32 bit ARM M33 MCU operating with 250 MHz clock, 2 MBytes of program flash memory and 640 KBytes of RAM.

Compared systems use 16nm AMD ZynqUltrascale+ device with 64 bit ARM A53 Microprocessor and programmable logic in the same device and Petalinux OS.

- Low-cost systems have an AMD ZynqUltrascale+ device and DDR4 with all peripheral interfaces soldered on a single, low cost PCB
- Module-based systems have an AMD ZynqUltrascale+ device and DDR4 soldered on an 4x5 cm module connected by connectors to a carrier board with all peripheral interfaces



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1.1 Low cost systems used by UTIA in EECONE T4.3 and T4.4

| [1] | STM32H573I-DK | https://www.st.com/en/evaluation- tools/stm32h573i-dk.html | Local or remote system control (www-server or secure mqtt client) for [2], [3] |
|-----|-------------------|--|--|
| [2] | TE0802-02-1BEV2-A | https://shop.trenz- electronic.de/en/TE0802-02- 1BEV2-A-MPSoC-Development- Board-with-AMD-Zyng-UltraScale- ZU1EG-and-1-GB-LPDDR4?c=474 | AMD Vitis AI 3.0 AMD DPU in PL USB camera, remote X11 desktop |
| [3] | TE0802-02-2AEV2-A | MPSoC Development Board mit AMD Zyng™ UltraScale+™ ZU2 und 1 GB LPDDR4 Trenz Electronic GmbH Online Shop (EN) (trenz-electronic.de) | AMD Vitis AI 3.0 AMD DPU in PL USB camera, remote X11 desktop |





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1.2 Module based systems used by UTIA in EECONE T4.3 and T4.4

| [1] | STM32H573I-DK | https://www.st.com/en/evaluation- | Local or remote |
|-----|--------------------------|-------------------------------------|---------------------|
| | | tools/stm32h573i-dk.html | system control |
| | | | (www-server or |
| | | | secure mqtt client) |
| | | | for 2-1, 2-2 |
| | TE0701-06 | https://shop.trenz- | Carrier Board for |
| | Carrier Board for Trenz | electronic.de/en/TE0701-06- | range of 4x5 cm |
| | Electronic 4 x 5 Modules | Carrier-Board-for-Trenz-Electronic- | modules [3], [4]. |
| | TE0821 or TE0820 | <u>4-x-5-Modules?c=261</u> | |
| [4] | TE0821 Module: | https://shop.trenz- | AMD Vitis AI 3.0 |
| | | electronic.de/en/Products/Trenz- | AMD DPU in PL |
| | 17 module types | Electronic/TE08XX-Zynq- | USB camera |
| | (to be supported) | UltraScale/TE0821-Zynq- | remote X11 |
| | | UltraScale/ | desktop |
| [5] | TE0820 Module: | https://shop.trenz- | AMD Vitis AI 3.0 |
| | | electronic.de/en/Products/Trenz- | AMD DPU in PL |
| | 100 module types | Electronic/TE08XX-Zynq- | USB camera |
| | (to be supported) | UltraScale/TE0821-Zyng- | remote X11 |
| | | UltraScale/ | desktop |





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This application note [5] and the accompanying evaluation package describe support for systems based on TE0820 modules. It is available for free public download from UTIA server dedicated to UTIA contributions to EECONE project: https://zs.utia.cas.cz/index.php?ids=projects/eecone

It will be also available for free public download in format of an wiki tutorial on Trenz Electronic wiki server:

https://wiki.trenz-

<u>electronic.de/display/PD/Vitis+AI+and+Vitis+Acceleration+Tutorials+with+Trenz+Electronic+Modules</u>

1.3 Objective of This Application Note and Evaluation Package

This application note and the accompanying evaluation package describe system [5].

This application note describes how to design custom HW platform with AMD DPU for Vitis 2022.2 AI 3.0 inference for family of Trenz Electronic modules TE0820 with AMD Zynq Ultrascale+ device.

This application note [5] is using AMD Vitis 2022.2 and PetaLinux 2022 tools installed on Ubuntu 20.04. The described configuration integrated AMD DPU IP, version v4.1.0, with architecture DPUCZDX8G.

Described board configuration can operate as small standalone computer with 1 Gb Ethernet connectivity, and remote X11 desktop. Support package for this application note will be available for public download from [5].

The installed AMD DPU configurations require recompilation of Vitis AI 3.0 examples and inference models in the Vitis AI framework. This compilation process will be described in separate application note [6].

This application supports family of TE0820 modules listed in next tables with ID 15 to 115.

Process will be demonstrated on these two TE0820 module examples:

- ID=84 module: TE0820-05-4DE21MA, device xczu4ev-sfvc784-1-e, 2GB DDR4
- ID=106 module: TE0820-05-2AE21MA, device xczu2cg-sfvc784-1-e, 2GB DDR4

Module TE0820-05-4DE21MA has four A53 ARM cores and contains Bram and also URAM blocks in the PL part of the device. Therefore, it is possible to implement all possible configurations of the AMD DPU (from B512 up to B4096) in PL. Implementation of B4096 is demonstrated. Module requires integration on carrier board TE0701-06 due to higher requirements DC/DC converters.

Module TE0820-05-2AE21MA has only two A53 ARM cores and contains only BRAM blocks in relatively small PL part of the device. Therefore, it is possible to implement configuration of the AMD DPU from B512 to B1024. Implementation of B1024 is demonstrated. This module has signoficantly lower power consumption in comparison to TE0820-05-4DE21MA and allows integration on carrier board TE0701-06 or carrier board TE0707-02. It is compact carrier board with limited DC/DC capabilities.

Specification for each module ID defined in TE0820_board_files.csv file is input to the Vivado 2022.2 HW bring-up scripts. It is provided by the company Trenz Electronic. It is part



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of package provided by Trenz Electronic for supported family of modules TE0820 for AMD Vivado 2022.2 design flows.

List of supported TE0820 modules is reprinted from TE0820_board_files.csv file included in the evaluation package associated to this application note.

This application note and associated evaluation package enables support for "second-life" of **100** types of TE0820.

A module from this mighed has been used originally in another context which might become obsolete. We provide support to reuse this module again in large and challenging range of Vitis AI 3.0 HW accelerated inference applications.

| | | | | | | | DCD D | DDR | FLACE | EM |
|----|--------------------|----------------------|-----------------------------------|--------------|-----------------------|---------------------------------------|--------------|------|---------------|---------|
| ID | PRODID | DARTNAME | ROARDNAME | SHOPTNAME | | | PCB_R | _SIZ | FLASH SIZE | NIC_ |
| 15 | TE0920 02 04EV 1EA | YOTHANIE | trong bigito0820 dow 10:part0:2.0 | Any 10 3rb | achi v8 dual parallol | mt25gu512 gcpi x8 dual parallel | EV DEV/02 | 200 | _312E | AGR |
| 15 | TE0820-03-04EV-TEA | xczu4ev-sivc784-1-e | trenz biz:te0820_4ev_1e.part0:2.0 | 4ev_1e_2go | dsbi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | REV03 | 200 | 1201010 | 400 |
| 17 | TE0820-03-02CG-TEA | xczu2cg-sivc784-1-e | trenz biz:te0820_20g_1e:part0:2.0 | 20g_1e_2g0 | dsbi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | REV03 | 200 | 1201010 | 400 |
| 10 | TE0820-03-02EG-1EA | xczu2eg-sivc784-1-e | trenz biz:te0820_2eg_1e.part0:2.0 | 2eg_1e_2g0 | dsbi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 400 |
| 10 | TE0820-03-02EG-TEL | xczu2eg-sivc784-1-e | trenz biz:te0820_2eg_1e.part0:2.0 | 2eg_1e_2g0 | dsbi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 400 |
| 20 | TE0820-03-03CG-TEA | xczudog cfuc794-1-e | trenz bizte0820_scg_te.part0:2.0 | Acg 10 2gb | dsbi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 400 |
| 20 | TE0820-03-04CG-TEA | xczu4cg-sivc784-1-e | trenz biz:te0820_4cg_1e:part0:2.0 | 40g_1e_2g0 | dsbi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 400 |
| 21 | TE0820-03-03EG-1EA | xczu2og cfvc784-1-e | trenz biz:te0820_3eg_1e:part0:2.0 | Seg_1e_2gb | dspi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 400 |
| 22 | TE0820-03-03EG-TEL | xczu3eg-sivc784-1-e | trenz bizto0820_3eg_1e.part0:2.0 | 3eg_1e_2g0 | dspi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 400 |
| 23 | TE0820-03-2A121FA | xczu2cg-sivc784-1-1 | trenz biz:te0820_20g_10;part0:2.0 | 20g_11_2g0 | dspi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 900 |
| 24 | TE0820-03-28E21FE | xczu2eg-sivc784-1-e | trenz bizto0820_2eg_1e.part0:2.0 | 2eg_1e_2g0 | dspi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | OGP |
| 25 | TE0920-03-341210A | xczu3cg-sivc784-1-1 | trenz biz:te0820_3cg_10;part0:2.0 | 20g 10 2gb | dspi-x8-dual_parallel | mt25qu512 qspi-x8-dual_parallel | PEV/02 | 200 | 1201010 | 9GD |
| 20 | TE0820-03-38E21FA | xczu3eg-sivc784-1-e | trenz bizte0820_3eg_1e.part0.2.0 | Jeg_1e_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | DEV03 | 200 | 120100 | 000 |
| 27 | TE0820-03-3BE21FL | xczuSeg-SIVC704-1-e | trenz bizite0820_3eg_1e.part0.2.0 | Seg_ie_zgo | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 20 | TE0820-03-02CG-1ED | xczu2cg-sivc784-1-e | trenz bizite0820_20g_1e.part0:2.0 | 2cg_ie_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 25 | TE0820-03-2AE21FA | xczu2cg-siVC784-1-e | trenz bizite0820_20g_1e.part0.2.0 | 2cg_ie_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 21 | TE0820-03-28E21FA | xczu2eg-sivc784-1-e | trenz bizite0820_2eg_1e.part0.2.0 | 2eg_1e_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 22 | TE0820-03-3AL21FA | xczu3cg-sivc784-1-e | trenz bizite0820_3cg_1e.part0.2.0 | 3cg_1e_2go | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 32 | TE0820-03-5A121FA | xczubcg-sivc784-1-1 | trenz bizite0820_scg_10.part0.2.0 | Acg_10_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 24 | TE0820-03-4AE21FA | xczu4cg-sivc784-1-e | trenz bizite0820_4cg_1e.part0.2.0 | 4cg_1e_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 25 | TE0820-03-4DE21FA | xczu4ev-sivc784-1-e | trenz bizito0820_4ev_1e.part0:2.0 | 4ev_1e_2gb | qspi-xo-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REVUS | 200 | 1201010 | OGD OCD |
| 26 | TE0920-02-4DE21E | xczu4ev-sivc784-1-0 | trenz biz:te0820_4ev_11:part0:2.0 | 4ev_11_2g0 | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | PEV/02 | 200 | 120100 | 800 |
| 27 | TE0820-03-4DE21FC | xczu4ev-sivc784-1-e | trenz biz:te0820_4ev_1e:part0:2.0 | 4ev_1e_2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | PEV/02 | 200 | 120100 | 800 |
| 20 | TE0920-02-4A121EL | xczu4ev-sivc784-1-i | trenz biz:te0820_4ev_1e.part0:2.0 | 4ev_1e_2go | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | PEV/02 | 200 | 120100 | 900 |
| 20 | TE0920-02-5DP21EA | x22u4cg-51VC784-1-1 | trenz biz:te0820_40g_11.part0.3.0 | 50v 1g 2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | PEV/02 | 200 | 120100 | 900 |
| 40 | TE0920-02-20121EA | xazu3ev-sivc784-1Q-q | trenz biz:te0820_3ev_1q.part0:2.0 | 20g 1i 2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | PEV/02 | 200 | 120100 | 900 |
| 40 | TE0920-02-2012114 | xczu2eg-sivc784-1-i | trenz biz:te0820_2eg_1i.part0:2.0 | 2eg_11_2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | PEV/02 | 200 | 120100 | 900 |
| 41 | TE0820-03-2DI21FA | xczu2eg-51vc784-1-i | trenz biz:te0820_2eg_11:part0:2.0 | 5ev 1i 2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV03 | 20B | 128MB | 8GB |
| 42 | TE0820-04-24E21E4 | xczu2cg.sfvc784-1-0 | trenz biz:te0820_2cg_le:nart0:2.0 | 2cg 1e 2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | SGB |
| 43 | TE0820-04-2A121EA | xczu2cg_stvc784_1_i | trenz bizte0820_2cg_1c.putto2.0 | 2cg_1c_2g5 | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | SGB |
| 45 | TE0820-04-28E21EA | xczu2eg 51vc764-1-0 | trenz biz:te0820_2eg_1e:part0:2.0 | 205_11_250 | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | SGB |
| 46 | TE0820-04-28E21EA1 | xczu2eg-sfvc784-1-e | trenz biz:te0820_2eg_1e:part0:2.0 | 2eg_1e_2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 47 | TE0820-04-28E21EI | xczu2eg-sfvc784-1-e | trenz biz:te0820_2eg_1e:part0:2.0 | 2eg_1e_2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 48 | TE0820-04-28E21-V1 | xczu2eg-sfvc784-1-e | trenz biz:te0820_2eg_1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 49 | TE0820-04-2BI21EA | xczu2eg-sfvc784-1-i | trenz biz:te0820_2eg_1i:part0:2.0 | 2eg_10_2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 50 | TE0820-04-2BI21FI | xczu2eg-sfvc784-1-i | trenz biz:te0820_2eg_1i:part0:2.0 | 2eg 1i 2gb | gspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 51 | TE0820-04-3AE21EA | xczu3cg-sfvc784-1-e | trenz.biz:te0820_3cg_1e:part0:2.0 | 3cg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 52 | TE0820-04-3AI21FA | xczu3cg-sfvc784-1-i | trenz.biz:te0820_3cg_li:part0:2.0 | 3cg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 53 | TE0820-04-3AI21FAT | xczu3cg-sfvc784-1-i | trenz.biz:te0820_3cg_li:part0:2.0 | 3cg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 54 | TE0820-04-3BE21FA | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 55 | TE0820-04-3BE21FL | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 56 | TE0820-04-3BE21KA | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 64GB |
| 57 | TE0820-04-4AE21FA | xczu4cg-sfvc784-1-e | trenz.biz:te0820 4cg 1e:part0:2.0 | 4cg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 58 | TE0820-04-4AI21FI | xczu4cg-sfvc784-1-i | trenz.biz:te0820 4cg 1i:part0:3.0 | 4cg 1i x 2gb | qspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 59 | TE0820-04-4BI21KL | xczu4eg-sfvc784-1-i | trenz.biz:te0820 4eg 1i:part0:2.0 | 4eg 1i 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 64GB |
| 60 | TE0820-04-4DE21FA | xczu4ev-sfvc784-1-e | trenz.biz:te0820 4ev 1e:part0:2.0 | 4ev 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| | | | | v | | · · · · · · · · · · · · · · · · · · · | | | | |



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| 61 | TE0820-04-4DE21FL | xczu4ev-sfvc784-1-e | trenz.biz:te0820_4ev_1e:part0:2.0 | 4ev_1e_2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
|-------|--------------------|----------------------|-----------------------------------|--------------|-----------------------|---------------------------------|-------|------|---------------|------|
| 62 | TE0820-04-4DI21FA | xczu4ev-sfvc784-1-i | trenz.biz:te0820_4ev_1i:part0:2.0 | 4ev_1i_2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 63 | TE0820-04-5DI21FA | xczu5ev-sfvc784-1-i | trenz.biz:te0820_5ev_1i:part0:2.0 | 5ev_1i_2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 64 | TE0820-04-5DR21FA | xazu5ev-sfvc784-1Q-q | trenz.biz:te0820_5ev_1q:part0:2.0 | 5ev_1q_2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 65 | TE0820-04-3BE21ML | xczu3eg-sfvc784-1-e | trenz.biz:te0820_3eg_1e:part0:2.0 | 3eg_1e_2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 66 | TE0820-04-4DE21MA | xczu4ev-sfvc784-1-e | trenz.biz:te0820_4ev_1e:part0:2.0 | 4ev 1e 2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 67 | TE0820-04-4DI21MA | xczu4ev-sfvc784-1-i | trenz.biz:te0820_4ev_1i:part0:2.0 | 4ev 1i 2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 68 | TE0820-04-S002 | xczu3eg-sfvc784-1-e | trenz.biz:te0820_3eg_1e:part0:2.0 | 3eg 1e 2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 69 | TE0820-04-S005 | xczu4cg-sfvc784-1-e | trenz.biz:te0820_4cg_1e:part0:2.0 | 4cg_1e_2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 70 | TE0820-04-S004 | xczu2eg-sfvc784-1-e | trenz.biz:te0820_2eg_1e:part0:2.0 | 2eg 1e 2gb | qspi-x8-dual_parallel | mt25qu512-qspi-x8-dual_parallel | REV04 | 2GB | 128MB | 8GB |
| 71 | TE0820-04-2BE21MA | xczu2eg-sfvc784-1-e | trenz.biz:te0820 2eg 1e:part0:2.0 | 2eg 1e 2gb | qspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 72 | TE0820-04-S006 | xczu4ev-sfvc784-1-e | trenz.biz:te0820 4ev 1e:part0:2.0 | 4ev 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 73 | TE0820-04-2BI21ML | xczu2eg-sfvc784-1-i | trenz.biz:te0820 2eg 1i:part0:2.0 | 2eg 1i 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 74 | TE0820-04-S002C1 | xczu2eg-sfvc784-1-e | trenz.biz:te0820 2eg 1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 75 | TE0820-04-S003 | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 76 | TE0820-04-S009 | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 77 | TE0820-04-S010 | xczu4ev-sfvc784-1-e | trenz.biz:te0820 4ev 1e:part0:2.0 | 4ev 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 78 | TE0820-04-4AE21MA | xczu4cg-sfvc784-1-e | trenz.biz:te0820 4cg 1e:part0:2.0 | 4cg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 79 | TE0820-04-2BE21MAJ | xczu2eg-sfvc784-1-e | trenz.biz:te0820 2eg 1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 80 | TE0820-04-3BE21MLZ | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 81 | TE0820-04-S013 | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 82 | TE0820-04-S016 | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 83 | TE0820-05-4BI21PLZ | xczu4eg-sfvc784-1-i | trenz.biz:te0820 4eg 1i:part0:2.0 | 4eg 1i 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 64GB |
| 84 | TE0820-05-4DE21MA | xczu4ev-sfvc784-1-e | trenz.biz:te0820 4ev 1e:part0:2.0 | 4ev 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 85 | TE0820-05-S002C1 | xczu4cg-sfvc784-1-e | trenz.biz:te0820 4cg 1e:part0:2.0 | 4cg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 86 | TE0820-05-S003 | xczu4ev-sfvc784-1-e | trenz.biz:te0820 4ev 1e:part0:2.0 | 4ev 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 87 | TE0820-05-S004C1 | xczu2eg-sfvc784-1-e | trenz.biz:te0820 2eg 1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 88 | TE0820-05-S008C1 | xczu2eg-sfvc784-1-e | trenz.biz:te0820_2eg_1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 89 | TE0820-04-S018 | xczu4cg-sfvc784-1-e | trenz.biz:te0820 4cg 1e:part0:2.0 | 4cg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 90 | TE0820-05-2AE21MA7 | xczu2cg-sfvc784-1-e | trenz.biz:te0820_2cg_1e:part0:2.0 | 2cg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 91 | TE0820-05-3BE21MA7 | xczu3eg-sfvc784-1-e | trenz.biz:te0820_3eg_1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 92 | TE0820-05-S014C1 | xczu4cg-sfvc784-1-e | trenz.biz:te0820_4cg_1e:part0:2.0 | 4cg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 93 | TE0820-04-5DI21MA | xczu5ev-sfvc784-1-i | trenz.biz:te0820_5ev_1i:part0:2.0 | 5ev 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 94 | TE0820-05-4BI21PI | xczu4eg-sfvc784-1-i | trenz.biz:te0820_4eg_1i:part0:2.0 | 4eg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 64GB |
| 95 | TE0820-05-S016 | xczu3eg-sfvc784-1-e | trenz.biz:te0820_3eg_1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 96 | TE0820-04-2BI21MA | xczu2eg-sfvc784-1-i | trenz.biz:te0820_2eg_li:part0:2.0 | 2eg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 97 | TE0820-05-3BE21MA | xczu3eg-sfvc784-1-e | trenz.biz:te0820_3eg_1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 98 | TE0820-05-S013 | xczu2eg-sfvc784-1-e | trenz.biz:te0820_2eg_1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 99 | TE0820-05-2AI81MA | xczu2cg-sfvc784-1-i | trenz.biz:te0820_2cg_li:part0:2.0 | 2cg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 100 | TE0820-05-3BI21ML | xczu3eg-sfvc784-1-i | trenz.biz:te0820 3eg 1i:part0:2.0 | 3eg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 101 | TE0820-04-2AI21MC | xczu2cg-sfvc784-1-i | trenz.biz:te0820_2cg_li:part0:2.0 | 2cg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV04 | 2GB | 128MB | 8GB |
| 102 | TE0820-05-2BI81ML | xczu2eg-sfvc784-1-i | trenz.biz:te0820_2eg_li:part0:2.0 | 2eg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 103 | TE0820-05-S022 | xczu3cg-sfvc784-1-e | trenz.biz:te0820 3cg 1e:part0:2.0 | 3cg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 104 | TE0820-05-2BE21MA | xczu2eg-sfvc784-1-e | trenz.biz:te0820_2eg_1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 105 | TE0820-05-4AI21MI | xczu4cg-sfvc784-1-i | trenz.biz:te0820 4cg 1i:part0:3.0 | 4cg 1i x 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 106 | TE0820-05-2AE21MA | xczu2cg-sfvc784-1-e | trenz.biz:te0820_2cg_1e:part0:2.0 | 2cg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 107 | TE0820-05-2AI21MA | xczu2cg-sfvc784-1-i | trenz.biz:te0820_2cg_1i:part0:2.0 | 2cg 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 108 | TE0820-05-2BE21MAJ | xczu2eg-sfvc784-1-e | trenz.biz:te0820_2eg_1e:part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 109 | TE0820-05-3AE21MA | xczu3cg-sfvc784-1-e | trenz.biz:te0820 3cg 1e:part0:2.0 | 3cg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 110 | TE0820-05-3BE81MI | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e;part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual_parallel | REV05 | 2GB | 128MB | 8GB |
| 111 | TE0820-05-4DI21MA | xczu4ev-sfvc784-1-i | trenz.biz:te0820_4ev_1i:part0:2.0 | 4ev 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual_parallel | REV05 | 2GB | 128MB | 8GB |
| 112 | TE0820-05-5DI81MA | xczu5ev-sfvc784-1-i | trenz.biz:te0820_5ev_1i:part0:2.0 | 5ev 1i 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual_parallel | REV05 | 2GB | 128MB | 8GB |
| 113 | TE0820-05-S017C1 | xczu2eg-sfvc784-1-e | trenz.biz:te0820_2eg_1e;part0:2.0 | 2eg 1e 2gb | gspi-x8-dual parallel | mt25gu512-gspi-x8-dual_parallel | REV05 | 2GB | 128MB | 8GB |
| 114 | TE0820-05-S020 | xczu3eg-sfvc784-1-e | trenz.biz:te0820 3eg 1e:part0:2.0 | 3eg 1e 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| 115 | TE0820-05-5DI21MA | xczu5ev-sfvc784-1-i | trenz.biz:te0820 5ev 1i:part0:2.0 | 5ev 1i 2gb | gspi-x8-dual parallel | mt25qu512-qspi-x8-dual parallel | REV05 | 2GB | 128MB | 8GB |
| | | | | | | derer debt vie ener beitungt | | 000 | | EA.4 |
| | | | | | | | DCD 0 | DUR | EL A CU | EIVI |
| D | PRODID | DARTNAME | POARDNAME | SHOPTHANAS | | | PCB_R | _312 | rLASH SIZE | |
| 0 | PRODU | PADUNAIVIE | DUADUNAIVIE | | LC LINUFLASTI ITP | FEGALASTITE | | 16 | - 3IZE | JALE |

Supported TE0820 modules with ID = 15 ... 115

2 Prepare Reference Design for Extensible Custom Platform

The design proces is demonstrated for module with ID=84: TE0820-05-4DE21MA, device xczu4ev-sfvc784-1-e, 2GB DDR4. If your module has different ID, replace 84 with that ID.

In Ubuntu terminal, source paths to Vitis and Vivado tools by

```
$ source /tools/Xilinx/Vitis/2022.2/settings64.sh
```

Download TE0820 test_board Linux Design file(see Reference Design download link on chapter <u>Requirements</u>) with pre-build files to

department of signal processing

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https://sp.utia.cas.cz



This TE0820 test_board ZIP file contains bring-up scripts for creation of Petalinux for range of modules in zipped directory named "test_board".

Unzip the file to directory:

```
~/work/te0820 84 240
```

All supported modules are identified in file:

```
~/work/te0820 84 240/test board/board files/TE0820 board files.csv
```

We will select module 84 with name TE0820-05-4DE21MA, with device xczu04ev-sfvc784-1e on TE0701-06 carrier board. We will use default clock 240 MHz. That is why we name the package te0820_84_240 and proposed to unzip the TE0820 test_board Linux Design files into the directory:

~/work/te0820_84_240

2.1 Reference HW for TE0820 module

In Ubuntu terminal, change directory to the test_board directory:

```
$ cd ~/work/te0820_84_240/test_board
```

Setup the test_board directory files for a Linux host machine. In Ubuntu terminal, execute:

\$ chmod ugo+rwx ./console/base sh/*.sh

```
$ chmod ugo+rwx ./_create_linux_setup.sh
```

```
$ ./ create linux setup.sh
```

Select option (0) to open Selection Guide and press Enter





| ,∓1 | devel@ubuntu: ~/work/te0820_84_240/test_board | Q | Ξ | | | × |
|--|---|-------------------------------------|-----------------------------|------------------------------|---------------|------------|
| settings devel@ut sh devel@ut p.sh devel@ut Run [Use [| 564.sh puntu:~/work/te0820_84_240/test_board\$ chmod ugo+rw puntu:~/work/te0820_84_240/test_board\$ chmod ugo+rw puntu:~/work/te0820_84_240/test_board\$./_create_li puntu:~/work/te0820_84_240/test_board\$./_create_li posign with: _create_linux_setup.sh posign Path: /home/devel/work/te0820_84_240/test_bo | /x ./ /x ./ .nux_ pard | conso _crea setup | le/bas te_lir .sh - | e_sh nux_s | /*. etu |
| | create_linux_setup.cmdTE Reference Design | | | - | | |
| (d) (x) (0) (1) (2) (3) (3) (a) | Go to Documentation (Web Documentation) Exit Batch (nothing is done!) Module selection guide, project creation Create minimum setup of CMD-Files and exit Batch Create maximum setup of CMD-Files and exit Batch (internal only) Dev Install Board Files from Xilinx Board Store (beta) Start design with unsupported Vivado Version (bet (ex.:'0' for module selection guide): | :a) | | | | |

Select variant 84 from the selection guide, press enter and agree selection

| F | de | evel@ubunt | u: ~/work/te0 | 820_84_240/te | st_board | | | | | × |
|---|--|---|---|--|-----------------------------------|------------------|--------|------|---------------|-----|
| For better | table v | iew please | e resize wi | ndows to fu | ll screer | n! | | | | |
| Select Mod | ule will | be done i | in 2 steps: | | | | | | | |
| Step 1: (se -Change mod -Display ce -Restore w -Reduce Li er step is -Reduce Li -Reduce Li -Reduce Li -Reduce Li -Reduce Li -Reduce Li -Reduce Li | elect co dule lis urrent mode st by ID bypassed st by Ar st by So st by PC st by DD st by Fl st by EM st by Ot st by No out seled | Lumn filte t size (fo odule list ule list, press: ' d and id r ticle Numb C/FPGA, pr REV, press AC, press: ash, press MC, press tes, press tion, press | er): or small mo c, press: 'R' ID' or 'id number is u per, press: ess: 'FPGA ess: 'PCB' 'DDR' or ' c' FLASH' c' FLASH' s: 'FLASH' s: 'OTHERS s: 'NOTES' ess: 'Q' or | nitors only L' or 'l' or 'r' ' or insert sed) 'AN' or 'a ' or 'fpga' or 'pcb' ddr' or 'pcb' ddr' or 'flash' 'emmc' ' or 'other or 'notes' 'q' |), press: ID colur n' s' | : 'fu' nns va | ll' or | 'sma | all' tly(f | ilt |
| Please Ento 84 | er Optio | 1: | | | | | | | | |

Create Vivado Project with option 1

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| ŪTIA | Akademie věd České republiky Ústav teorie informace a automatizace AV ČR, v.v.i. | | © 2024 ÚTIA AV ČR, v.v.i. All disclosure and/or reproduction rights reserved |

| ΓŦ | devel@ubuntu: ~/work/t | e0820_84_240/l | est_board | J Q ≡ | | | × |
|---|---|------------------------|-----------|------------------------|-------|-------|----------|
| Step 2: Insert I | D: | | | | | | |
| ID Product ID B REV | SoC/FPGA Ty Notes | /p DDR Size | Flash | SHORT DIR Size EMMC | Size | 0ther | PC 's |
| 84 TE0820-05-4 V05 | DE21MA xczu4ev-sfv Other EMMC mfr | /c784-1-e 2GB - | 128MB | 4ev_1e_2g 8GB | ь | NA | RE |
| You like to star y What would you l - Create and ope - Create vivado - Both, press 2 | t with this device? y ike to do? n delivery binary fo project, press 1 | //N Lder, press | 0 | | | - | |

Vivado Project will be generated for the selected variant.

3 HW support for Vitis Extensible Design Flow

3.1 Create Extensible platform HW

This section describes manual creation of extensible platform HW. You can follow it or you can alternatively use the fast track script described in section 3.2.

In Vivado project, click in **Flow Navigator** on **Settings**. In opened Settings window, select **General** in **Project Settings**, select **Project is an extensible Vitis platform**. Click on **OK**.





IP Integrator of project set up as an extensible Vitis platform has an additional Platform Setup window.

Add multiple clocks and processor system reset IPs

In IP Integrator Diagram Window, right click, select **Add IP** and add **Clocking Wizard** IP **clk_wiz_0**. Double-click on the IP to Re-customize IP window. Select Output Clocks panel. Select four clocks with frequency 100, 200, 400 and 240 MHz.

100 MHz clock will serve as low speed clock.

200 MHz and 400 MHz clock will serve as clock for AMD DPU AI 3.0 HW IP.

240 MHz clock will serve as the default extensible platform clock. By default, Vitis will compile HW IPs with this default clock.

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Set reset type from the default Active High to **Active Low**.



| A Vivado - | | | | | A | Ja 28 06:5 | 3 | | | | | | | A | to () |
|----------------------|--------------------------|------------|------------------|------------|-----------------|------------|-----------|--------------------|-------|-------------------|---------------|------|--------|--------------------|-------|
| | | | | | Recustomize | 10 | | | | | | 0 | | | |
| File Edit Flow To | | | | | Re-coatoninze | | | | | | | | | | Ready |
| | Clocking Wizard (6.0) | | | | | | | | | | | A | | III Default Lavout | neady |
| low Navigator | | | | | | | | | | | | | | | |
| PROJECT MANAGER | Documentation Generation | ation | | | | | | | | | | | | | 2.0 |
| Settings | IP Symbol Besource | | Companyet Name | elle mit 0 | | | | | | | | | | | ° u |
| Add Sources | Show disabled ports | | Component Name | cik_wig_0 | | | | | | | | | | | |
| Language Template | C | | Clocking Options | Output | t Clocks MMC | 4 Setting | s Summary | | | | | | | | |
| 후 IP Catalog | | | Clk out1 | clk_out1 | 100.000 | - 6 | 100.00000 | 0.000 | 0.0 | 00 | 50.000 | 0 ^ | Memory | | |
| PINTEGRATOR | | | Clk_out2 | clk_out2 | 200.000 | 6 | 200.00000 | 0.000 | © 0.0 | 00 | 50.000 | 0 | | | |
| Create Block Design | | | Clk_out3 | clk_out3 | @ 400.000 | G | 400.00000 | 0.000 | © 0.0 | 00 | 50.000 | 01 | | | |
| pen Block Design | | | Clk out4 | clk_out4 | 240.000 | 0 | 240.00000 | 0.000 | © 0.0 | 00 | 50.000 | 0 | | | |
| Generate Block Des | | | Clk out5 | clk out5 | 100.000 | | | 0.000 | | | 50.000 | | | | |
| Export Platform | | | Clk out6 | clk_out6 | 100.000 | | | 0.000 | | | 50.000 | | | | |
| | | | Ck out7 | clk out7 | 100.000 | | | 0.000 | | | 50.000 | _ | | | |
| JLATION | | | | | | | | | | | - | _ | | | |
| The Contractory | | cik_out1 | Thuse concerse | OUENCING | | | | | | | | - 11 | | | |
| TL ANALYSIS | • resetn | clk_out2 | | | | | | | | | | - 11 | - | | |
| Open Elaborated D4 | - clk_in1 | clk_out3 - | Output Cloc | k Sequ | uence Number | | | | | | | - 11 | | | |
| NTHESIS | | clk_out4 | | 1 | | | | | | | | - 11 | | | |
| Run Synthesis | | locked - | | 1 | | | | | | | | - 11 | - | | |
| Open Synthesized D | | | | 1 | | | | | | | | - 11 | _ | ? | - 0 1 |
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| PLEMENTATION | | | | 1 | | | | | | | | - 11 | | | 1 |
| Open Implementation | | | | 1 | | | | | | | | - 11 | | | |
| operimpented | | | | | | | | | | | | | | | |
| ROGRAM AND DEBUG | | | Fachly Only and | | | | Deces T | | | the second second | | | | | |
| 👫 Generate Bitstream | | | Enable Optional | inputs / c | Jucputs for MMC | M/PLL | Reset Ty | Je | P | nase shirt | Mode | | | | |
| Open Hardware Mar | | | ereset [|] power_do | own 🗌 input_cl | <_stopped | () Ac | tive High (Active | e Low | O WAVE | FORM () LATEN | CY Y | | | |
| | | | | | | | | | | | | | | | , |

Clik on OK to close the Re-customize IP window.

Connect input **resetn** of **clk_wiz_0** with output **pl_resetn0** of **zynq_ultra_ps_e_0**. Connect input **clk_in1** of **clk_wiz_0** with output **pl_clk0** of **zynq_ultra_ps_e_0**.



Add and connect four Processor System Reset blocks for each generated clock.





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Open Platform Setup window of IP Integrator to define Clocks. In Settings, select Clock.

In "Enabled" column select all four defined clocks **clk_out1**, **clk_out2**, **clk_out3**, **clk_out4** of **clk_wiz_0** block.

In "ID" column keep the default Clock ID: 1, 2, 3, 4

In "Is Default" column, select **clk_out4** (with ID=4) as the default clock. One and only one clock must be selected as default clock.

| <u>P</u> layer • | - 号 [1] 汉 | | | | | | | | | ~ | 1 5 |
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| Activities | 🙏 Vivado 🕶 | | Au | g 28 07:00 | | | | | | A 40 (| |
| - | | test_board - [/h | ome/devel/work/te0820_84_2 | 40/test_board/vivado/test_board.xpr] - Vivado 2022.2 | | | | | | | |
| ·🕑 | Elle Edit Flow Tools Rep | ogits Window Layout View Help Q. Quick Access | | | | | | | _ | Read | dy |
| _ | | X . T . H . X . X . X | | | | | | | II De | ault Layout | ~ |
| | Flow Navigator # 0 ? _ | BLOCK DESIGN - ZUSYS * | | | | | | | | 1.1 | ? > |
| | V PROJECT MANAGER | | and the second second second | | | | | | | | |
| | Settings | Sources Design x Signais Board ? _ [] | Address Editor X Addre | ss Map X Platform Setup X | | | | | | 7 L | 1 12 |
| | Add Sources | Q 7 14 Q | Settings | Clock | | | | | | | |
| | Language Templates | a ck_out2 | AXI Port | | | | | | | | |
| (?) | 👎 IP Catalog | clk_out3 | | | Freehlad | 10 | in Defender de | Deres Rui | Charles . | | _ |
| - | | ∝ clk_out4 | All Stream Port | v e util ds buf 0 (Utility Buffer 2.2) | Enabled | 10 | Is Default | Proc Sy | Status | Freque | |
| | V IP INTEGRATOR | ∉ locked | 4 Clock | IBUF OUT | | | | | | | |
| | Create Block Design | ⇒ resetn | ✓ Interrupt | # zyng ultra ps e 0 (Zyng UltraScale+ MPSoC:3.4) | | | | | | | |
| | Open Block Design | > # itag_axe_0 (ITAG to AXI Master:1.2) | Platform Name | pl_clk0 | D | | | | | | |
| > | Concernts Direct Decise | s abtools_rmeter_0 (Labtools Frequency Counter VI.0:1.0) | | \$\sigma \vert clk_wiz_0 (Clocking Wizard: 6.0) | | | | | | | |
| | Generate Block Design | < | | clk_out1 | 2 | 1 | 0 | /proc_s | fixed | ✓ 100 MHz | |
| | Export Platform | Platform Interface Properties ? _ 	 II II × | | clk_out2 | 1 | 2 | | /proc_s | fixed | ✓ 200 MHz | |
| | | Platform interface Properties P = 0.0 x | | clk_out3 | | 3 | | /proc_s | fixed | ✓ 400 MHz | |
| | SIMULATION | 🖹 clk_out4 🔶 👄 🗢 | | clk_out4 | | :4 | ۲ | /proc_s | fixed | ✓ 240 MHz | |
| | Run Simulation | Name, clk out t | | | | | | | | | |
| | | Harres Cis_Guid | | | | | | | | | |
| | RTL ANALYSIS | Type: Clock | | Info: No problems with Clock interfaces. | | | | | | | |
| | > Open Elaborated Design | C Enabled | | • | | | | | | | |
| | SYNTHESIS | General Options | Export Platform | | | | | | | | |
| | Run Synthesis | Tel Cancola y Macrogan Log Reports Derion R | une l | | | | | | | 2 5 | |
| | > Open Synthesized Design | O T A H D R R | 4115 | | | | | | | 7 - 6 | 1.11 |
| | | Ч±♥∥⊎⊞ш | | | | | | | | | |
| | IMPLEMENTATION | <pre>set_property PFM.CLOCK {clk_out1 {id "2" is_default "fal set_property PFM.CLOCK {clk_out1 {id "2" is_default "fal</pre> | lse" proc_sys_reset "/proc_sys lse" proc_sys_reset "/proc_sys | reset_1" status "fixed" freq hz '100000000') clk_out2 (id reset_1" status "fixed" freq hz '100000000') clk_out2 (id | "3" is_def | ault "false ault "false | proc_sys_ | reset "/pri | <pre>/c_sys_res /c_sys_res</pre> | et_2" status "fi set 2" status "fi | 12 |
| | Run Implementation | set_property PFM.CLOCK {clk_out1 {id "2" is_default "fal | lse" proc_sys_reset "/proc_sys | reset_1" status "fixed" freq_hz "100000000"} clk_out2 {id | "3" is_def | ault "false | proc_sys | reset "/pri | xc_sys_rer | et_2" status "fi | i) |
| | > Open Implemented Design | <pre>set_property pfm_name zusys iget_files (zusys.bd); set property PFM.CLOCK (clk out) (id "1" is default "fal</pre> | ise" proc sys reset "/proc sys | reset 1" status "fixed" freg hz "100000000") clk out2 (id | "3" is def | ault "false | " proc sys | reset "/pr | | set 2" status "f" | is i |
| | | set_property PFM.CLOCK {clk_outl {id "1" is_default "fal | lse" proc_sys_reset "/proc_sys | reset 1' status "fixed" freq hz '100000000'} clk_out2 {id | "3" is_def | ault "false | proc_sys | reset "/pri | c_sys_rer | et_2" status "fi | 1> |
| | PROGRAM AND DEBUG | set property PFM.CLOCK (clk outl (1d "1" is default "fal set property PFM.CLOCK (clk outl (id "1" is default "fal | lse" proc_sys_reset "/proc_sys lse" proc_sys_reset "/proc_sys | reset 1" status "fixed" freq hz "100000000"} clk_out2 (id reset 1" status "fixed" freq hz "100000000"} clk_out2 (id | "2" 15_def | ault false | <pre>proc_sys proc_sys</pre> | reset "/pri | <pre>>>C_sys_res >>> sys_res</pre> | et_2" status "fi | 12 |
| | III Generate Bitstream | set_property PFM.CLOCK {clk_out1 {id "1" is_default "fal | lse" proc_sys_reset "/proc_sys | reset_1" status "fixed" freq_hz "100000000"} clk_out2 (id | "2" 1s_def | ault false | proc_sys | reset "/pri | c_sys_rer | iet_2" status "fi | 12 |
| | | set property PFM.CLOCK {clk_outl {id "1" is default "fall set property PFM.CLOCK {clk_outl {id "1" is default "fall | lse" proc_sys_reset "/proc_sys lse" proc_sys_reset "/proc_sys | reset 1' status "fixed" freq hz '100000000'} clk out2 (id reset 1' status "fixed" freq hz '100000000'} clk out2 (id | "2" 15_def | ault "false | proc_sys | reset "/pri | IC_SYS_FES | et_2" status "fr | 1) |
| | Open Hardware Manager | set_property PFM.CLOCK {clk_outl {id "1" is_default "fal | lse" proc_sys_reset "/proc_sys | reset_1" status "fixed" freq_hz "100000000"} clk_out2 (id | "2" is_def | ault "false | proc_sys | reset "/pri | c_sys_res | et_2" status "fi | 15 |
| | | 1 | | | | | | | | | ~ |
| | | Type a Tcl command here | | | | | | | | | - |
| | | | | | | | | | | | |

Double-click on **zynq_ultra_ps_e_0** block and enable **M_AXI_HPM0_FPD** port. Select data width 32bit. It will be used for integration of inerrupt controller on new dedicated AXI stream subsystem with 240 MHz clock. It will also enable new input

pin maxihpm0_fpd_aclk of zynq_ultra_ps_e_0. Connect it to 240 MHz clock net.

| signal processing | | https://sp.utia.cas.cz |
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Connect input pin **maxihpm0_fpd_aclk** of **zynq_ultra_ps_e_0** to the 240 MHz **clk_out4** of **clk_wiz_0** IP block.



Add, customize and connect the AXI Interrupt Controller

Add AXI Interrupt Controller IP **axi_intc_0**. Double-click on **axi_intc_0** to re-customize it.

In "Processor Interrupt Type and Connection" section select the "Interrupt Output Connection" from "Bus" to "Single".

Click on OK to accept these changes.

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| | | | | 🔛 Default Layout 🗸 🗸 |
| • | Flow Navigator 🗧 🤉 🔤 | AXI Interrupt Controller (4.1) | A | • ? × |
| | V PROJECT MANAGER | O Documentation 🗁 IP Location | | 2 🗆 🖒 |
| A | Settings | | | |
| _ | Add Sources | Show disabled ports | Component Name axi_intc_0 | |
| 2 | IR Catalon | | | 1 |
| | + ii catalog | | Basic Advanced Clocks | Sy Status Freque |
| | ✓ IP INTEGRATOR | | Interrupt Usage | |
| 2 | Create Block Design | | Number of Peripheral Interrupts (Auto) 1 V | |
| | Open Block Design | | Fast Interrupt Mode | |
| • | Generate Block Design | | Enable Fast Interrupt Logic | s fixed 🗸 100 MHz |
| | Export Platform | | Interrupt Vector Address reset value (Auto) 0x00000000000000000000000000000000000 | s fixed v 200 MHz |
| | V SIMULATION | | | s fixed v 240 MHz |
| | Run Simulation | + s axi | Peripheral Interrupts Type | |
| | PTI ANALYSIS | s axi aclk | auro Interrupts type - Edge or Level 0xFFFFFFF 0 | |
| | > Open Elaborated Design | irq — | Auto Level type - High or Low 0xFFFFFFF 0 | |
| | | - intro.01 | | |
| | ✓ SYNTHESIS | | Edge type - Rising or Falling 0xFFFFFFF 0 | |
| | Run Synthesis | | | ? _ 🗆 🖾 |
| | Open Synthesized Design | | | |
| | ✓ IMPLEMENTATION | | Processor Interrupt Type and Connection | /proc_sys_reset_2" status "fi) ~ |
| | Run Implementation | | Interrupt type | /proc_sys_reset_2" status "fi> |
| | > Open Implemented Design | | Level type Active High 🗸 | /proc_sys_reset_2" status "fi> |
| | Y PROGRAM AND DEBUG | | Interrupt Output Connection Single V | |
| | III Generate Bitstream | | | |
| | > Open Hardware Manager | | | |
| | | | | |
| | | | OK | > |
| | | | | |
| | | | | |



Connect interrupt controller clock input **s_axi_aclk** of **axi_intc_0** to output **dlk_out4** of **clk_wiz_0**. It is the default, 240 MHz clock of the extensible platform.

Connect interrupt controller input **s_axi_aresetn** of **axi_intc_0** to

output **peripheral_aresetn[0:0]** of **proc_sys_reset_4**. It is the reset block for default, 240 MHz clock of the extensible platform.



Use the **Run Connection Automation** wizard to connect the axi lite interface of interrupt controller **axi_intc_0** to master interface **M_AXI_HPM0_FPD** of **zynq_ultra_ps_e_0**.



In Run Connection Automaton window, click OK.

New AXI interconnect **ps_8_axi_periph** is created. It connects master interface **M_AXI_HPM0_FPD** of **zynq_ultra_ps_e_0** with interrupt controller **axi_intc_0**.



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| | Processor System Reset Pag_all_0 Object Object Pag_all_0 Object < | |
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Double-click on **zynq_ultra_ps_e_0** to re-customize it by enabling of an interrupt input **pl_ps_irq0[0:0]**. Click OK.

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| • 🕑 1 | File Edit Flow Tools Res | | | | | Re-customize IP | | | Rer | adv |
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| | Language Templates | | • 0 × • | | | | | | | |
| | 후 IP Catalog | Switch To Advanced Mode | | | | | āy | Status | Freque | |
| _ | V ID INTEGRATOR | PS UltraScale+ Block Design | Search: Q. | | | | | | | |
| 1 - Angel - An | Create Block Design | VO Configuration | Name × General | Sele | ct | | | | _ | |
| - | Open Block Design | | Interrupts | | | | | | | |
| | Generate Block Design | Clock Configuration | V PL to PS | | | | | | | |
| | Export Platform | DDR Configuration | IRQ0[0-7] | 1 | \sim | | s | fixed 🗸 | 100 MHz | |
| | Export Platform | PE PL Configuration | IRQ1[0-7] | 0 | \sim | | s | fixed ~ | 200 MHz | |
| | ✓ SIMULATION | P 5 P C Conliguration | APU Legacy Interrupts(IRI | Q 🗆 | | | .s | fixed v | 400 MH2 | |
| | Run Simulation | | RPU Legacy Interrupts(IRI | Q 🗆 | | | | | 2401416 | |
| | | | > PS to PL | | | | | | | |
| | ✓ RTL ANALYSIS | | > Fabric Reset Enable | 1 | | | | | | |
| | > Open Elaborated Design | | > Address Fragmentation | | | | | | | _ |
| | | | > Others | | | | | | | |
| | ✓ SYNTHESIS | | > PS-PL Interfaces | | | | | | | _ |
| | Run Synthesis | | > Debug | | | | | | | - |
| | > Open Synthesized Design | | | | | | r | | 7 = | 06 |
| | ✓ IMPLEMENTATION | | | | | | | | | ^ |
| | Run Implementation | | | | | | | | | |
| | > Open Implemented Design | | | | | | | | | |
| | Y PROGRAM AND DEBUG | | | | | | | | | |
| | III Generate Bitstream | | | | | | | | | |
| | > Open Hardware Manager | | | | | |)} Ma | ster {/zynd | _ultra_ps_e | 0,0 |
| | | | | | | | | | | |
| ::: | | | | | | OK Cancel | F | | | > |
| | | 4 | | - | - | | | | | |

Modify the automatically generated reset network of AXI interconnect **ps_8_axi_periph** .

Disconnect input **S00_ARESETN** of **ps_8_axi_periph** from the network driven by output **peripherial_aresetn[0:0]** of **proc_sys_reset_4** block.

Connect input **S00_ARESETN** of **ps_8_axi_periph** block with output **interconnect_aresetn[0:0]** of **proc_sys_reset_4** block.



Disconnect input **M00_ARESETN** of **ps_8_axi_periph** block from the network driven by output **peripherial_aresetn[0:0]** of **proc_sys_reset_4** block.

Connect input **M00_ARESETN** of **ps_8_axi_periph** to output **interconnect_aresetn[0:0]** of **proc_sys_reset_4** block.

This modification will make the reset structure of the AXI interconnect **ps_8_axi_periph** block identical to the future extensions of this interconnect generated by the Vitis extensible design flow.

Connect the interrupt input pl_ps_irq0[0:0] of zynq_ultra_ps_e_0 block with output irq of axi_intc_0 block.



In Platform Setup, select "Interrupt" and enable intr in the "Enabled" column.





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UTTA Akade Ústav Rename automatically generated name **ps8_0_axi_periph** of the interconnect to new name: **axi_interconnect_1**. This new name will be used in Platform Setup selection of AXI ports for the extensible platform.

In Platform Setup, select AXI Ports for zynq_ultra_ps_e_0:

Select M_AXI_HPM1_FPD in column "Enabled".

Select **S_AXI_HPC0_FPD** and **S_AXI_HPC1_FPD** in column "Enabled".

For **S_AXI_HPC0_FPD**, change S_AXI_HPC to **S_AXI_HP** in column "Memport".

For **S_AXI_HPC1_FPD**, change S_AXI_HPC to **S_AXI_HP** in column "Memport".

Select S_AXI_HP0_FPD, S_AXI_HP1_FPD, S_AXI_HP2_FPD, S_AXI_HP3_FPD in column "Enabled".

Type into the "sptag" column the names for these 6 interfaces so that they can be selected by v++ configuration during linking phase. **HPC0**, **HPC1**, **HP0**, **HP1**, **HP2**, **HP3**



In "Platform Setup", select AXI Ports for the recently renamed axi_interconnect_1:

Select **M01_AXI, M02_AXI, M03_AXI, M04_AXI, M05_AXI, M06_AXI** and **M07_AXI** in column "Enabled".

Make sure, that you are selecting these AXI ports for the 240 MHz AXI interconnect **axi_interconnect_1**

Keep all AXI ports of the 100 MHz interconnect axi_interconnect_0 unselected. The AXI interconnect axi_interconnect_0 connects other logic and IPs which are part of the initial design.



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| Platform Setup | | | | | | | ? _ 5 |
| | | | | | | | |
| Settings | AXI Port | | | | | | |
| ✓ AXI Port | ¥ 🗢 🔳 | | | | | | |
| AXI Stream Port | Name | Enabled | Memport | | SP Tag | Memory | |
| Clock | M_AXI_HPM1_FPD | 8 | M_AXI_GP | ~ | ~ | | |
| | S_AXI_HPC0_FPD | 1 | S_AXI_HP | ~ | HPC0 v | | |
| Interrupt | S_AXI_HPC1_FPD | × | S_AXI_HP | ~ | HPC1 v | | |
| ✓ Platform Name | S_AXI_HP0_FPD | 2 | S_AXI_HP | ~ | HP0 v | | |
| | S_AXI_HP1_FPD | | S_AXI_HP | ~ | HP1 v | | |
| | S_AXI_HP2_FPD | 2 | S_AXI_HP | ~ | HP2 v | | |
| | S_AXI_HP3_FPD | 2 | S_AXI_HP | ~ | HP3 v | | |
| | S_AXI_LPD | | | | | | |
| | ✓ I axi interconnect 1 (AXI Interconnec | t:2.1) | | | | | |
| | S01 AXI | | | | | | |
| | = S02 AXI | 0 | | | | | |
| | = 503 AXI | 0 | | | | | |
| _ | S04 AXI | 0 | | | | | |
| | = 505 AXI | 0 | | | | | |
| | = 506 AX | 0 | | | | | |
| | = S07 AVI | 0 | | | | | |
| | = 508 AX | 0 | | | | | |
| | = S00 AVI | | | | | | |
| | = \$10 AV | 0 | | | | | |
| | = 510_000 | | | | | | |
| | = C12 AV | | | | | | |
| | = \$12_M | | | | | | |
| | E 014 AV | | | | | | |
| | | | | | | | |
| | MOL AVI | | M AVE GR | | | | |
| | MO2_AVI | • | M_AXLCD | × | · · | | |
| | MO2_AM | e (| M_AXLOP | ~ | ~ | | |
| | NO4 AV | e | M_AXLOP | ~ | ~ | | |
| | | • | M_ANI_OP | ~ | ~ | | |
| | MOS_ANI | Sec. | M_AXLOP | ~ | ~ | | |
| | M05_A0 | × | M_AVLOP | ~ | ~ | | |
| | E M07_40 | | M_AUL_GP | ~ | ~ | | |
| | MO8_AXI | U | | | | | |
| | Info: No problems with AXI Port interface | es. | | | | | |
| :: | | | | | | | |
| Export Platform | | | | | | | |

The modifications of the default design for the extensible platform are completed, now.

In Vivado, save block design by clicking on icon "Save Block Design".

Continue the design path with <u>Validate Design</u>.

To continue the manual design path, go to section 3.3 Validate design.

3.2 Fast Track for Creation of Extensible platform HW

HW modifications can be made by sourcing this script in Vivado with open diagram in IP Integrator.

Copy file from the accompanying support package

```
te0820_AI_3_0_eval_package\vivado\script_te0820.txt
```

to

```
~/work/te0820_84_240/test_board/vivado/script_te0820.txt
```

Execute in Vivado Tcl console this command:

source script te0820.txt

3.3 Validate Design

Results of HW creation via Manual Track or Fast Track are identical.

Open diagram by clicking on zusys.bd if not already open. In Diagram window, validate design by clicking on "Validate Design" icon.





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Received Critical Messages window indicates that input intr[0:0] of axi_intc_0 is not connected. This is expected. The Vitis extensible design flow will connect this input to interrupt outputs from generated HW IPs.

Click OK.

You can generate pdf of the block diagram by clicking to any place in diagram window and selecting "Save as PDF File". Use the offered default file name:

```
~/work/te0820 84 240/test board/vivado/zusys.pdf
```

3.4 Compile Created HW and Custom SW with Trenz Scripts

In Vivado Tcl Console, type following script and execute it by Enter. It will take some time to compile HW. HW design and to export the corresponding standard XSA package with included bitstream.

TE::hw_build_design -export_prebuilt

An archive for standard non-extensible system is created:

~/work/te0820 84 240/test board/vivado/test board 4ev 1e 2gb.xsa

In Vivado Tcl Console, type the following script and execute it by Enter. It will take some time to compile.

TE::sw run vitis -all

After the script controlling SW compilation is finished, the Vitis SDK GUI is opened.



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Close the Vitis "Welcome" page. Compile the two included SW projects. Standalone custom Vitis platform TE0820-05-4DE21MA has been created and compiled.



The TE0820-05-4DE21MA Vitis platform includes Trenz Electronic custom first stage boot loader in folder **zynqmp_fsbl**. It includes SW extension specific for the Trenz module initialisation.

This custom zynqmp_fsbl project has been compiled into executable file fsbl.elf. It is located in:

~/work/te0820_84_240/test_board/prebuilt/software/4ev_1e_2gb/fsbl.elf

This customised first stage boot loader is needed for the Vitis extensible platform. We have used the standard Trenz scripts to generate it for next use in the extensible platform.

Exit the opened Vitis SDK project.

In Vivado top menu select File->Close Project to close project. Click OK.

In Vivado top menu select File->Exit to close Vivado. Click OK.

The exported Vitis Extensible Hardware platform named test_board_4ev_1e_2gb.xsa can be found in the vivado folder.

3.5 Copy Created Custom First Stage Boot Loader

Up to now, test_board directory has been used for all development.

```
~/work/te0820 84 240/test board
```

Create new folders:

```
~/work/te0820_84_240/test_board_pfm/pfm/boot
~/work/te0820_84_240/test_board_pfm/pfm/sd_dir
```

signal processing

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Copy the recently created custom first stage boot loader executable file from

~/work/te0820 84 240/test board/prebuilt/software/4ev 1e 2gb/fsbl.elf

to

~/work/te0820_84_240/test_board_pfm/pfm/boot/fsbl.elf

4 Building Petalinux for Extensible Design Flow with Vitis AI 3.0 Support

4.1 Vitis AI 3.0 support

Download the Vitis-AI 3.0 repository. In browser, open page:

https://github.com/Xilinx/Vitis-AI/tree/3.0

Click on green Code button and download Vitis-AI-3.0.zip file. Unzip

Vitis-AI-3.0.zip

to directory ~/Downloads/Vitis-AI

Сору

~/Downloads/Vitis-AI

to ~/work/Vitis-AI-3.0

The directory

~/work/Vitis-AI-3.0

contains the Vitis-AI 3.0 framework, now.

To install the Vitis-AI 3.0 version of shared libraries into rootfs (when generating system image by PetaLinux) we have to copy recepies recipes-vitis-ai to the Petalinux project.

Сору

~/work/Vitis-AI-3.0/src/vai petalinux recepies/recipes-vitis-ai

to

~/work/te0802_04_240_vga/test_board/os/petalinux/project-spec/metauser/

Delete file:

~/work/te0802_04_240_vga/test_board/os/petalinux/project-spec/metauser/recipes-vitis-ai/vart/vart_3.0_vivado.bb

and keep only the unmodified file:

```
~/work/te0802_04_240_vga/test_board/os/petalinux/project-spec/meta-
user/recipes-vitis-ai/vart/vart_3.0.bb
```

signal processing

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File vart_3.0.bb will create vart libraries for Vitis design flow with dependency on the AMD xrt software framework.

4.2 Building Petalinux for Extensible Design Flow

Change directory to the default Trenz Petalinux folder

~/work/te0820 84 240/test board/os/petalinux

Source Vitis and Petalinux scripts to set environment for access to Vitis and PetaLinux tools.

\$ source /tools/Xilinx/Vitis/2022.2/settings64.sh

\$ source ~/petalinux/2022.2/settings.sh

Configure petalinux with the test_board_4ev_2gb.xsa for the extensible design flow by executing:

\$ petalinux-config --get-hw-description=

~/work/te0820_84_240/test_board/vivado

| .F1 | devel@ubuntu: ~/work/te0820_84_240/test_board/os/petali 🔍 🖃 – 🗆 😣 |
|-----|--|
| | me/devel/work/te0820_84_240/test_board/os/petalinux/project-spec/configs/con |
| ſ | <pre>misc/config System Configuration Arrow keys navigate the menu. <enter> selects submenus> (or empty submenus). Highlighted letters are hotkeys. Pressing <y> includes, <n> excludes, <m> modularizes features. Press <esc><to exit, <?> for Help, for Search. Legend: [*] built-in []</to </esc></m></n></y></enter></pre> |
| | -*- XYNQMP Configuration Linux Components Selection> Auto Config Settings> -*- Subsystem AUTO Hardware Settings> DTG Settings> PMUFW Configuration> FSBL Configuration> ARM Trusted Firmware Configuration> FPGA Manager> u-boot Configuration> Linux Configuration> Image Packaging Configuration> |
| - | Firmware Version Configuration> Yocto Settings> <select> < Exit > < Help > < Save > < Load ></select> |



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Select Exit->Yes to close this window.

In text editor, modify the user-rootfsconfig file:

~/work/te0820_86_240/test_board/os/petalinux/project-spec/metauser/conf/user-rootfsconfig

In text editor, append these lines:

#Note: Mention Each package in individual line #These packages will get added into rootfs menu entry CONFIG startup CONFIG webfwu CONFIG xrt CONFIG xrt-dev CONFIG zocl CONFIG opencl-clhpp-dev CONFIG opencl-headers-dev CONFIG packagegroup-petalinux-opencv CONFIG packagegroup-petalinux-opencv-dev CONFIG dnf CONFIG e2fsprogs-resize2fs CONFIG parted CONFIG resize-part CONFIG packagegroup-petalinux-vitisai CONFIG packagegroup-petalinux-self-hosted CONFIG cmake CONFIG packagegroup-petalinux-vitisai-dev CONFIG mesa-megadriver CONFIG packagegroup-petalinux-x11 CONFIG packagegroup-petalinux-v4lutils CONFIG packagegroup-petalinux-matchbox CONFIG packagegroup-petalinux-vitis-acceleration CONFIG packagegroup-petalinux-vitis-acceleration-dev CONFIG vitis-ai-library CONFIG vitis-ai-library-dev

signal processing





xrt, xrt-dev and zocl are required for Vitis acceleration flow. dnf is for package management. parted, e2fsprogs-resize2fs and resize-part can be used for ext4 partition resize.

Other included packages serve for natively building Vitis AI applications on target board and for running Vitis-AI demo applications with GUI.

The last three packages will enable use of the Vitis-AI 3.0 recepies for installation of the correspoding Vitis-AI 3.0 libraries into rootfs of PetaLinux.

Launch rootfs config:

```
$ petalinux-config -c rootfs
```

All packages will have to have an asterisk [*].

Only vitis-ai-library-dev and vitis-ai-library-dbg will stay indicated as unselected by: [].

Still in the RootFS configuration window, go to root directory by select Exit once.

Enable OpenSSH and Disable Dropbear

Dropbear is the default SSH tool in Vitis Base Embedded Platform. If OpenSSH is used to replace Dropbear, the system could achieve faster data transmission speed over ssh. Created Vitis extensible platform applications may use remote display feature. Using of OpenSSH can improve the display experience.

Go to Image Features. Disable ssh-server-dropbear and enable ssh-server-openssh and click Exit once.

Go to Filesystem Packages->misc->packagegroup-core-ssh-dropbear and disable packagegroup-core-ssh-dropbear.

Go to Filesystem Packages level by Exit twice.

Go to console->network->openssh and enable openssh, openssh-sftpserver, openssh-sshd, openssh-scp.

Go to root level by selection of Exit four times.

Enable Package Management

Package management feature can allow the board to install and upgrade software packages on the fly.

In rootfs config go to Image Features and enable

package management and debug_tweaks options. Click OK, Exit twice and select Yes to save the changes.

4.3 Disable CPU IDLE in Kernel Config

CPU IDLE would cause processors get into IDLE state (WFI) when the processor is not in use. When JTAG is connected, the hardware server on host machine talks to the processor

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regularly. If it talks to a processor in IDLE status, the system will hang because of incomplete AXI transactions.

So, it is recommended to disable the CPU IDLE feature during project development phase.

It can be re-enabled after the design has completed to save power in final products.

Launch kernel config:

\$ petalinux-config -c kernel

Ensure the following items are TURNED OFF by entering 'n' in the [] menu selection:

CPU Power Management->CPU Idle->CPU idle PM support

CPU Power Management->CPU Frequency scaling->CPU Frequency scaling

Exit and Yes to Save changes.

4.4 Add EXT4 rootfs Support

Let PetaLinux generate EXT4 rootfs. In terminal, execute:

\$ petalinux-config

Go to Image Packaging Configuration. Enter into Root File System Type

Select Root File System Type EXT4

Change the Device node of SD device from the default value /dev/mmcblk0p2

to new value required for the TE0820 module: /dev/mmcblk1p2

Step up to

Image Packaging Configuration -->

modify Root filesystem formats from

cpio cpio.gz cpio.gz.u-boot ext4 tar.gz jffs2

to

ext4

Exit and Yes to save changes.

4.5 Let Linux Use EXT4 rootfs During Boot

The setting of which rootfs to use during boot is controlled by bootargs. We would change bootargs settings to allow Linux to boot from EXT4 partition.

In terminal, execute:



\$ petalinux-config

Change DTG settings->Kernel Bootargs->generate boot args automatically to NO.

Update User Set Kernel Bootargs to:

```
earlycon console=ttyPS0,115200 clk_ignore_unused root=/dev/mmcblk1p2 rw
rootwait cma=512M
```

Click OK, Exit three times and Save.

4.6 Build PetaLinux Image

In terminal, build the PetaLinux project by executing:

\$ petalinux-build

The PetaLinux image files will be generated in the directory:

~/work/te0820 84 240/test board/os/petalinux/images/linux

Generation of PetaLinux takes some time and requires Ethernet connection and sufficient free disk space.

4.7 Create Petalinux SDK

The SDK is used by Vitis tool to cross compile applications for newly created platfom.

In terminal, execute:

\$ petalinux-build --sdk

The generated sysroot package sdk.sh will be located in directory

~/work/te0820 84 240/test board/os/petalinux/images/linux

Generation of SDK package takes some time and requires sufficient free disk space. Time needed for these two steps depends also on number of allocated processor cores.

4.8 Copy Files for Extensible Platform

Copy these four files:

| Files | From | То |
|---|---|--|
| bl31.elf pmufw.elf system.dtb u-boot- dtb.elf | ~/work/te0820_84_240/ test_board/os/petalinux/ images/linux | ~/work/te0820_84_240/ test_board_pfm/pfm/boot |

Rename the copied file u-boot-dtb.elf to u-boot.elf



The directory

~/work/te0820_84_240/test_board_pfm/pfm/boot

contains these five files:

bl31.elf fsbl.elf pmufw.elf system.dtb u-boot.elf

Copy files:

| Files | From | То |
|------------------------|---|--|
| boot.scr system.dtb | ~/work/te0820_84_240/ test_board/os/petalinux / images/linux | ~/work/te0820_84_240/ test_board_pfm/ pfm/sd_dir |

Copy file:

| File | From | То |
|---------|---|--|
| init.sh | ~/work/te0820_84_240/ test_board/misc/sd | ~/work/te0820_84_240/ test_board_pfm/pfm/sd_dir |

init.sh is an place-holder for user defined bash code to be executed after the boot:

```
#!/bin/sh
normal="\e[39m"
lightred="\e[91m"
lightgreen="\e[92m"
green="\e[32m"
yellow="\e[33m"
cyan="\e[36m"
red="\e[31m"
magenta="\e[95m"
echo -ne $lightred
echo Load SD Init Script
echo -ne $cyan
echo User bash Code can be inserted here and put init.sh on SD
echo -ne $normal
```

4.9 Create Extensible Platform zip File

Create new directory tree:



```
~/work/te0820 84 240 move/test board/os/petalinux/images
~/work/te0820 84 240 move/test board/Vivado
~/work/te0820 84 240 move/test board pfm/pfm/boot
~/work/te0820 84 240 move/test board pfm/pfm/sd dir
```

Copy all files from the directory:

| Files | Source | Destination |
|-----------------------------------|--|--|
| all | ~/work/te0820_84_240/test_b oard/os/petalinux/images | ~/work/te0820_84_240_move/tes t_board/os/petalinux/images |
| all | ~/work/te0820_84_240/test_b oard_pfm/pfm/boot | ~/work/te0820_84_240_move/tes t_board_pfm/pfm/boot |
| all | ~/work/te0820_84_240/test_b oard_pfm/pfm/sd_dir | ~/work/te0820_84_240_move/tes t_board_pfm/pfm/sd_dir |
| test_board _4ev_1e_2g b.xsa | ~/work/te0820_84_240/test_b oard/Vivado/test_board_4ev_ 1e_2gb.xsa | <pre>~/work/te0820_84_240_move/tes t_board/Vivado/test_board_4ev _1e_2gb.xsa</pre> |

Zip the directory

~/work/te0820 84 240 move

into ZIP archive:

~/work/te0820 84 240 move.zip

The archive te0820_84_240 move.zip can be used to create extensible platform on the same or on an another PC with installed Ubuntu 20.04 and Vitis tools, with or without installed Petalinux. The archive includes all needed components, including the Xilinx xrt library and the script sdk.sh serving for generation of the sysroot .

The archive has size approximately 3.6 GB and it is valid for the initially selected module number (84). This is the te0820 HW module with xczu4ev-sfvc784-1-e device with 2 GB memory. The extensible Vitis platform will have the default clock 240 MHz.

Move the te0820_84_240_move.zip file to an PC disk drive.

Delete: ~/work/te0820 84 240 move ~/work/te0820 84 240 move.zip

Clean the Ubuntu Trash.

4.10 Generation of SYSROOT

This part of development can be direct continuation of the previous Petalinux configuration and compilation steps.

Alternatively, it is also possible to implement all next steps on an Ubuntu 20.04 without installed PetaLinux Only the Ubuntu 20.04 and Vitis/Vivado installation is needed. All required files created in the PetaLinux for the specific module (24) are present in the archive: te0820 84 240 move.zip

In this case, unzip the archive to the directory:

~/work/te0820 84 240 move



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and copy all content of directories to ~/work/te0820_84_240

Delete the **te0820_84_240_move.zip** file and the **~/work/te0820_84_240_move** directory to save filesystem space.

In Ubuntu terminal, change the working directory to: ~/work/te0820 84 240/test board/os/petalinux/images/linux

In Ubuntu terminal, execute script enabling access to Vitis 2022.2 tools. Execution of script serving for setting up PetaLinux environment is not necessary:

\$ source /tools/Xilinx/Vitis/2022.2/settings64.sh

In Ubuntu terminal, execute script

\$./sdk.sh -d ~/work/te0820 84 240/test board pfm

SYSROOT directories and files for PC and for Zynq Ultrascale+ will be created in:

```
~/work/te0820_84_240/test_board_pfm/sysroots/x86_64-petalinux-linux
~/work/te0820_84_240/test_board_pfm/sysroots/cortexa72-cortexa53-
xilinx-linux
```

Once created, do not move these sysroot directories (due to some internally created paths).

4.11 Generation of Extensible Platform for Vitis

In Ubuntu terminal, change the working directory to:

```
~/work/te0820_84_240/test_board_pfm
```

Start the Vitis tool by executing

```
$ vitis &
```

In Vitis "Launcher", set the workspace for the extensible platform compilation:

~/work/te0820 84 240/test board pfm

Click on "Launch" to launch Vitis

Close Welcome page.

In Vitis, select in the main menu: File -> New -> Platform Project

Type name of the extensible platform: te0820_84_240_pfm. Click Next.

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Choose for hardware specification for the platform file:

~/work/te0820_84_240/test_board/vivado/test_board_4ev_1e_2gb.xsa

In "Software specification" select: linux

In "Boot Components" unselect Generate boot components (these components have been already generated by Vivado and PetaLinux design flow)

New window te0820_84_240_pfm is opened.

Click on linux on psu_cortex53 to open window Domain: linux_domain

In "Description" write: xrt

In "Bif File" find and select the pre-defied option: Generate Bif

In "Boot Components Directory" select: ~/work/te0820_84_240/test_board_pfm/pfm/boot

In "FAT32 Partition Directory" select: ~/work/te0820 84 240/test board pfm/pfm/sd dir



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| Image: platform.tcl Supported Runtimes: OpencL. Display Name: Imax on psu_cortexas33 Imax on psu_cortexas33 Description: xrt Imax on psu_cortexas40 Bif File: // home/devel/work/tco020_04_240/test_board_pfm/ Browse Boot Components Directory: // home/devel/work/tco020_04_240/test_board_pfm/ Browse | |
| Display Name: linux on psu_cortexa53 / Description: xrt / Bif File: //ome/devel/work/teo820_84_240/test_board_pfm// Browse Ru Boot Components.Directory: //ome/devel/work/teo820_84_240/test_board_pfm// Browse Q Ru | |
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| Bif File: //home/devel/work/te0820_84_240/test_board_pfm/ Browse Ru Boot Components Directory: //home/devel/work/te0820_84_240/test_board_pfm/ Browse Q Ru Hum Poolfr: Prome/devel/work/te0820_84_240/test_board_pfm/ Browse Q Ru | |
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| Sysred Directory: Brogse Q | |
| QEMU Data: //home/devel/work/teo820_94_240/test_board_pfm/l Browge Q Bin | |
| QEMU Arguments: /home/devel/work/te0820_84_240/test_board_pfm/i Browsg Q ha | |
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| platform write | |
| | |

In Vitis IDE "Explorer" section, click on te0820_84_240_pfm to highlight it.

Right-click on the highlighted te0820_84_240_pfm and select build project in the open submenu. Platform is compiled in few seconds. Close the Vitis tool by selection: File -> Exit.

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| | Main Hardware Specification | | (| | | | |
| | Console 21 Problems E Vitis Lo | n (i) Guidance | | A & & | 1.08.2 | | |
| | Build Concole (HoR20 94 240 pfm) 17:99:25 *** Build of project tel buildplatform.sh 33473 ted828 44 XSB Server Chamel: tcfchamel 17:39:39 Build Finished (took 13s | 2020 84 240 pfm **** 840 pfm **** 550ms) | | | | | |
| | | | | | | | |

Vits extensible platform te0820_84_240_pfm has been created in the directory:

~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_240_ pfm



5 Platform Usage

5.1 Read Platform Info

With Vitis environment setup, platforminfo tool can report XPFM platform information.

```
Platforminfo
~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_
240 pfm/te0820 84 240 pfm.xpfm
```

5.2 Create and Compile Vector Addition Example

 $Create new \ directory \ test_board_test_vadd \ to \ test \ Vitis \ extendable \ flow \ example \ ``vector \ addition"$

~/work/te0820 84 240/test board test vadd

Current directory structure:

```
~/work/te0820_84_240/test_board
~/work/te0820_84_240/test_board_pfm
~/work/te0820_84_240/test_board_test_vadd
```

Change working directory:

```
$cd ~/work/te0820_84_240/test_board_test_vadd
```

In Ubuntu terminal, start Vitis by:

```
$ vitis &
```

In Vitis IDE Launcher, select your working directory

~/work/te0820_84_240/test_board_test_vadd

Click on Launch to launch Vitis.

Select File -> New -> Application project. Click Next.

Skip welcome page if shown.

Click on [+ Add] icon and select the custom extensible platform te0820_84_240_pfm[custom] in the directory:

~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_ 240 pfm

We can see available PL clocks and frequencies. PL4 with 240 MHz clock is has been set as default in the platform creation process.

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Click Next.

In Application Project Details window type into Application project name: test_vadd Click Next.

In Domain window type (or select by browse):

Sysroot path:

```
~/work/te0820_84_240/test_board_pfm/sysroots/cortexa72-cortexa53-
xilinx-linux
```

Root FS:

```
~/work/te0820_84_240/test_board/os/petalinux/images/linux/rootfs.ext4
```

Kernel Image:

~/work/te0820_84_240/test_board/os/petalinux/images/linux/Image

Click Next.

In Templates window, if not done before, update Vitis IDE Examples and Vitis IDE Libraries.

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Select Host Examples:

In Find, type: vector add to search for the Vector Addition example.





Select: Vector Addition Click Finish New project template is created.

In test_vadd window menu "Active build configuration" switch from SW Emulation to Hardware.

In "Explorer" section of Vitis IDE, click on: test_vadd_system[te0820_84_240_pfm] to select it.

Right Click on: test_vadd_system[te0820_84_240_pfm] and select in the opened submenu: Build project

Vitis will compile. This step can take some time.





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Created extended HW with integrated vadd IP block can be open and analysed in Vivado 2022.2.

5.3 Run Compiled test_vadd Example Application

The sd_card.img file is output of the compilation and packing by Vitis. It is located in directory:

```
~/work/te0820_84_240/test_board_test_vadd/test_vadd_system/Hardware/pac
kage/sd card.img
```

Write the sd card image sd_card.img to SD card.

In Windows Pro 10 (or Windows 11 Pro) PC, inst all program Win32DiskImager for this task. Win32 Disk Imager can write raw disk image to removable devices. <u>https://win32diskimager.org/</u>

Insert the SD card to the TE0701-06 carrier board.

Connect PC USB terminal (115200 bps) card to the TE0701-06 carrier board.

Connect Ethernet cable to the TE0701-06 carrier board.

Power on the TE0701-06 carrier board.

signal processing

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In PC, find the assigned serial line COM port number for the USB terminal. In case of Win 10 use device manager.

In PC, open serial line terminal with the assigned COM port number. Speed 115200 bps.

On TE0701-06, reset button to start the system. USB terminal starts to display booting information.

In PC terminal, type:

```
sh-5.0# cd /media/sd-mmcblk1p1/
sh-5.0# ./test vadd krnl vadd.xclbin
```

The application test_vadd should run with this output:

```
INFO: Reading krnl_vadd.xclbin
Loading: 'krnl_vadd.xclbin'
Trying to program device[0]: edge
Device[0]: program successful!
TEST PASSED
sh-5.0#
```

The Vitis application has been compiled to HW and evaluated on custom system with extensible custom te0820_84_240_pfm platform.

In PC terminal type:

halt

System is halted. Messages relate to halt of the system can be seen on the USB terminal.

The SD card can be safely removed from the TE0701-06 carrier board, now.

The TE0701-06 carrier board can be disconnected from power.

System can be connected to the X11 terminal running on your PC Ubuntu with PuTTY application via Ethernet.

Find Ethernet IP address of your board by **ifconfig** command in PetaLinux terminal. In PC Ubuntu OS, open PuTTY application. In PuTTY, set Ethernet IP of your board. In PuTTY, select checkbox SSH->X11->Enable X11 forwarding.

Use PC Ubuntu mouse and keyboard. In PuTTY, open PetaLinux terminal and login as: user: root pswd: root.

In opened PetaLinux terminal, start X11 desktop x-session-manager by typing:

root@Trenz:~# x-session-manager &

Click on X11 icon (A Unicode capable rxvt)

signal processing

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Terminal opens as an X11 graphic window. In X11 terminal rxvt, use Ubuntu PC keyboard and type:

```
sh-5.0# cd /media/sd-mmcblk1p1/
sh-5.0# ./test vadd krnl vadd.xclbin
```

The application test_vadd should run with this output:

```
INFO: Reading krnl_vadd.xclbin
Loading: 'krnl_vadd.xclbin'
Trying to program device[0]: edge
Device[0]: program successful!
TEST PASSED
sh-5.0#
```

The test_board has been running the PetaLinux OS and drives simple version of an X11 GUI on Ubuntu desktop.Application test_vadd has been started from X11 xrvt terminal emulator.

Close the rxvt terminal emulator by click "x" icon (in the upper right corner) or by typing:

sh-5.0# exit

In X11, click Shutdown icon to safely close PetaLinux running on the test board.

System on the test board is halted. Messages related to halt of the system can be seen on the PC USB terminal.

The SD card can be safely removed from the test_board, now. Close the PC USB terminal application. The TE0701-06 carrier board can be disconnected from power, now.

6 Vitis AI 3.0 DPUCZDX8V_VAI_v3.0 Installation

This test implements simple AI 3.0 demo to verify DPU integration to our custom extensible platform. This tutorial follows Xilix Vitis Tutorial for zcu104 with necessary fixes and customizations required for our case.

We have to install correct Vitis project with the DPU instance from this repository:

https://github.com/Xilinx/Vitis-AI/tree/3.0/dpu

Page description contains table with supported targets. Use the line if theis table dedicated to DPUCZDX8G DPU for MPSoC and Kria K26 devices.

It is link for download of the programmable logic based DPU, targeting general purpose CNN inference with full support for the Vitis AI ModelZoo. Supports either the Vitis or Vivado flows on 16nm Zyng® UltraScale+™ platforms.

Click on the **Download** link in the column: Reference Design

This will result in download of file:

signal processing

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~/Downloads/DPUCZDX8V_VAI_v3.0.tar.gz

It contains direktory

~/Downloads/DPUCZDX8V VAI v3.0

Copy this directory to the directory:

~/work/DPUCZDX8V VAI v3.0

It contains HDL code for the DPU and also source files and project files to test the DPU with Al resnet50 inference example.

6.1 Create and Build Vitis Design

Create new directory test_board_dpu_trd to test Vitis extendable flow example dpu trd

~/work/te0820 84 240/test board dpu trd

Current directory structure:

```
~/work/te0820 84 240/test board
~/work/te0820 84 240/test board pfm
~/work/te0820 84 240/test board test vadd
~/work/te0820 84 240/test board dpu trd
```

Change working directory:

```
$cd ~/work/te0820 84 240/test board dpu trd
```

In Ubuntu terminal, start Vitis by:

\$ vitis &

In Vitis IDE Launcher, select your working directory

~/work/te0820 84 240/test board dpu trd

Click on Launch to start Vitis.

6.2 Add DPU Project template to the Vitis Extensible Flow

Open menu Window → Preferences

Go to Library Repository tab

Add Vitis-AI by clicking Add button and fill the form as shown below, use absolute path to your home folder in field Location



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| | | Guidance | Vitis Accelerated Libraries Repository | ID | vitis-ai | | |
| | | Library Repositorie | | Name | Vitis AI | | |
| _ | | Software Reposito | | | vitis AI 3.0 | | |
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| | Assistant 🗱 📟 | Additional General | | | | | |
| | | ▶ C/C++ | | Location | /home/devel | /work/DPUCZDX8G_V | /AI_v3.0 |
| | | Run/Debug | | Git URL | | | |
| | | r leall | | Branch | | | |
| | | | | | | | |
| | | | Add Remove | | | | |
| | | | | | | Restore Defaults | Apply |
| | | | | | | | |
| | | ? | | | | Cancel Ap | oply and Close |
| | 0 items selected | | | | | | r |
| | | | absolute path to your home directory. It dep | ends on the use | er name. The u | ser name in the figure | is "devel". Replace il |
| | | | by your user name. | | | | |
| | | Corr | ectly added library appears in Libraries: | | | | |
| | | Ope | n menu Xilinx → Libraries | | | | |
| | | O You | can find there just added Vitis-AI library mark | ed as "Installed" | ' as shown in in | nage: | |
| ::: | | » | MI - W (o) SM (o | 1948 • Heli Vela DE | | | |
| | | - | 0-00 0-00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | Access - | - • | A 2 Deep & Deep | |

Click Apply and Close.

Field Location says that the Vitis-AI repository from github has been allready cloned into

~/work/DPUCZDX8V_VAI_v3.0

folder, in the stage of Petalinux configuration. Use the absolute path to your home directory. It depends on the user name. The user name in the figure is "devel". Replace it by your user name.

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Correctly added library appears in Libraries:

Open menu Xilinx → Libraries...

You can find there just added Vitis-AI library marked as Installed



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6.3 Configure Project for the Vitis Extensible Flow with DPU

Select File -> New -> Application project. Click Next.

Skip welcome page, if it is shown.

Click on [+ Add] icon and select the custom extensible platform te0820_84_240_pfm[custom] in the directory:

~/work/te0820_84_240/test_board_pfm/te0820_84_240_pfm/export/te0820_84_240_ pfm

We can see available PL clocks and frequencies. PL4 with 240 MHz clock was set as the default in the platform creation process.



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Click Next.

In Application Project Details window type into Application project name: dpu_trd Click Next.

In Domain window type (or select by browse):

"Sysroot path":

```
~/work/te0820_84_240/test_board_pfm/sysroots/cortexa72-cortexa53-
xilinx-linux
```

"Root FS":

```
~/work/te0820 84 240/test board/os/petalinux/images/linux/rootfs.ext4
```

"Kernel Image":

~/work/te0820 84 240/test board/os/petalinux/images/linux/Image

Click Next.

In Templates window, if not done before, update Vitis IDE Examples and Vitis IDE Libraries

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In "Find", type: dpu to search for the DPU Kernel (RTL Kernel) example.

Select: DPU Kernel (RTL Kernel)







Click Finish

New project template is created.

In dpu_trd window menu Active build configuration switch from SW Emulation to Hardware

File dpu_conf.vh located at dpu_trd_kernels/src/prj/Vitis directory contains DPU configuration.

Open file dpu_conf.vh and change in line 37: `define URAM_DISABLE

to `define URAM ENABLE

and save modified file.

In case of module with ID=106 module: TE0820-05-2AE21MA, device xczu2cg-sfvc784-1-e use this new content of file dpu_conf.vh to specify DPU with 1024 and use of BRAMs.

```
* Copyright 2019 Xilinx Inc.
*
* Licensed under the Apache License, Version 2.0 (the "License");
signal processing
https://sp.utia.cas.cz
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```



```
* you may not use this file except in compliance with the License.
* You may obtain a copy of the License at
   http://www.apache.org/licenses/LICENSE-2.0
* Unless required by applicable law or agreed to in writing, software
* distributed under the License is distributed on an "AS IS" BASIS,
* WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or
implied.
* See the License for the specific language governing permissions and
* limitations under the License.
*/
//Setting the arch of DPU, For more details, Please read the PG338
/*===== Architecture Options =====*/
// |------|
// | Support 8 DPU size
// | It relates to model. if change, must update model
// +-----+
// | `define B512
// +-----+
// | `define B800
// +-----+
// | `define B1024
// +-----+
// | `define B1152
// +-----+
// | `define B1600
// +-----+
// | `define B2304
// +-----+
// | `define B3136
// +-----+
// | `define B4096
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```

ŪTĬA

//_|------| `define B1024 // |-----| // | If the FPGA has Uram. You can define URAM EN parameter // | if change, Don't need update model // +-----+ // | for zcu104 : `define URAM ENABLE // +-----+ // | for zcu102 : `define URAM DISABLE // |-----| `define URAM DISABLE //config URAM `ifdef URAM ENABLE `define def UBANK IMG N 5 `define def UBANK WGT N 17 `define def UBANK BIAS 1 `elsif URAM DISABLE `define def UBANK IMG N 0 `define def UBANK WGT N 0 `define def UBANK BIAS 0 `endif // |-----| // | You can use DRAM if FPGA has extra LUTs // | if change, Don't need update model // +-----+ // | Enable DRAM : `define DRAM ENABLE // +-----+ // | Disable DRAM : `define DRAM DISABLE // |-----| `define DRAM DISABLE signal processing

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//config DRAM `ifdef DRAM ENABLE `define def DBANK IMG N 1 `define def DBANK WGT N 1 `define def DBANK BIAS 1 `elsif DRAM DISABLE `define def DBANK IMG N 0 `define def DBANK WGT N 0 `define def DBANK BIAS 0 `endif // |------| // | RAM Usage Configuration // | It relates to model. if change, must update model // +-----+ // | RAM Usage High : `define RAM USAGE HIGH // +-----+ // | RAM Usage Low : `define RAM USAGE LOW // |------| `define RAM USAGE LOW // |------| // | Channel Augmentation Configuration // | It relates to model. if change, must update model // +-----+ // | Enable : `define CHANNEL AUGMENTATION ENABLE // +-----+ // | Disable : `define CHANNEL AUGMENTATION DISABLE // |------| `define CHANNEL AUGMENTATION ENABLE // |-----| // | ALU parallel Configuration signal processing https://sp.utia.cas.cz 45/62



// | It relates to model. if change, must update model // +-----+ // | setting 0 : `define ALU PARALLEL DEFAULT // +-----+ // | setting 1 : `define ALU PARALLEL 1 // |-----| // | setting 2 : `define ALU_PARALLEL_2 // |------| // | setting 3 : `define ALU PARALLEL 4 // |------| // | setting 4 : `define ALU PARALLEL 8 // |------| `define ALU PARALLEL DEFAULT // +-----+ // | CONV RELU Type Configuration // | It relates to model. if change, must update model // +-----+ // | `define CONV RELU RELU6 // +-----+ // | `define CONV RELU LEAKYRELU RELU6 // |------| `define CONV RELU LEAKYRELU RELU6 // +-----+ // | ALU RELU Type Configuration // | It relates to model. if change, must update model // +-----+ // | `define ALU RELU RELU6 // +-----+ // | `define ALU RELU LEAKYRELU RELU6 // |-----|

`define ALU_RELU_RELU6



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| <pre>// </pre> | signal processing | https://sp.utia.cas.c |
| <pre>// </pre> | // | |
| <pre>// </pre> | define LOWPOWER_DISABLE | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE // `define SAVE_ARGMAX_ENABLE // // DSP48 Usage Configuration // Use dsp replace of lut in conv operate // if change, Don't need update model // ++ // `define DSP48_USAGE_HIGH // ++ // `define DSP48_USAGE_LOW // `define DSP48_USAGE_HIGH // </pre> | | |
| <pre>// </pre> | // | |
| <pre>// </pre> | // `define LOWPOWER_DISABLE | |
| <pre>// </pre> | // ++ | |
| <pre>// </pre> | // tt | |
| <pre>// </pre> | // if change, Don't need update model | |
| <pre>// argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // </pre> | // Power Configuration | |
| <pre>// </pre> | // | |
| <pre>// </pre> | `define DSP48_USAGE_HIGH | |
| <pre>// </pre> | // | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // </pre> | // `define DSP48_USAGE_LOW | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE // // DSP48 Usage Configuration // Use dsp replace of lut in conv operate // if change, Don't need update model // ++ // `define DSP48_USAGE_HIGH</pre> | // ++ | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE // // DSP48 Usage Configuration // Use dsp replace of lut in conv operate // if change, Don't need update model // ++</pre> | // `define DSP48_USAGE_HIGH | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE // </pre> | // ++ | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE // // DSP48 Usage Configuration // Use dsp replace of lut in conv operate</pre> | <pre>// if change, Don't need update model</pre> | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE // // DSP48 Usage Configuration</pre> | // Use dsp replace of lut in conv operate | |
| <pre>// argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE_ARGMAX_ENABLE</pre> | // DSP48 Usage Configuration | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // `define SAVE ARGMAX ENABLE</pre> | ······································ | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE // </pre> | `define SAVE ARGMAX ENABLE | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++ // disable : `define SAVE_ARGMAX_DISABLE</pre> | // | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE_ARGMAX_ENABLE // ++</pre> | // disable : `define SAVE_ARGMAX_DISABLE | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // ++ // enable : `define SAVE ARGMAX ENABLE</pre> | // ++ | |
| <pre>// // argmax or max Configuration // It relates to model. if change, must update model // </pre> | // t | |
| <pre>// // argmax or max Configuration // argmax or max Configuration</pre> | <pre>// It relates to model. if change, must update model // </pre> | |
| // | // argmax or max Configuration | |
| | <pre>// // argmax or max Configuration</pre> | |

| // | | DEVICE Configuration |
|----|----|------------------------------------|
| // | | if change, Don't need update model |
| // | +- | + |
| // | | `define MPSOC |
| // | +- | + |
| // | | `define ZYNQ7000 |
| // | - | I |
| | | |

`define MPSOC

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| Activities | s 🚽 Vitis IDE 🔫 | Aug 18 11:18 | 👬 🌒 🕛 👻 |
| • 🍅 • 📄 🛕 ? | S File Edit Search Xilinx Project Wind C | tarterKlt_test_dpu_trd - test_dpu_trd_kernels/src/prj/Vitis/dpu_conf.vh - Vitis IDE tow Help | Pesign Pebug Debug Debug |
| · · · | | 40// 41 42 'define B4096 43 44// | |
| | test_dpu_trd_system [System] test_dpu_trd_system_iwv_link [Hw femulation-SW [Software Emulat dpu OPUCZDX8G [User Manage sfm_xrt_top [User Manage femulation-HW [Hardware Emula dpu OPUCZDX8G [User Manage sfm_xrt_top [User Manage sfm_xrt_top [User Manage sfm_xrt_top [User Manage dpu OPUCZDX8G [User Manage sfm_xrt_top [User Manage sfm_xrt_top [User Manage sfm_xrt_top [User Manage sfm_xrt_top [User Manage | S8 'define def UBANK_NOTN 17 59 'define def UBANK_NOTN 17 59 'define def UBANK_BTAS 1 60 'elsif URAM DISABLE 6 61 'define def UBANK_MGTN 0 62 'define def UBANK_MGTN 0 63 'define def UBANK_BTAS 0 64 'endif © Console ⊠ Problems © Vitis Log ① Guidance □ □ | ₩ 10 8 |
| | | | |

This modification is necessary for successful implementation of the DPU on the zcu04-ev module with internal memories implemented in URAMs.

Go to dpu_trd_system_hw_link and double click on dpu_trd_system_hw_link.prj

Remove sfm_xrt_top kernel from binary container by right clicking on it and choosing remove.

Reduce number of DPU kernels to one.

| signar | department of processing | https://sp.utia.cas.cz |
|--------|---|---|
| | 48/6 | 62 |
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6.4 Configure Connection of DPU kernel

On the same tab right click on dpu and choose Edit V++ Options

20_04_Vitis_2022_2_Petalinux_te0808_15eg_4gb_lattice - VMware Workstation 16 Player



Click "..." button on the line of V++ Configuration Settings and modify configuration as follows:

```
[clock]
freqHz=20000000:DPUCZDX8G 1.aclk
freqHz=40000000:DPUCZDX8G 1.ap clk 2
[connectivity]
sp=DPUCZDX8G 1.M AXI GP0:HPC0
sp=DPUCZDX8G 1.M AXI HP0:HP0
sp=DPUCZDX8G 1.M AXI HP2:HP1
```

Build the test_dpu_trd Project 6.5

In "Explorer" section of Vitis IDE, click on:

```
dpu trd system[te0802 04 240 vga pfm]
```

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to select it. Right Click on:

```
dpu_trd_system[te0802_04_240_vga_pfm]
```

and select in the opened sub-menu: Build project

Compilation takes some time (approximately 30 minutes).

Created extended HW with integrated DPU with configuration B4096 can be open and analysed in Vivado 2022.2



7 Prepare SD card with test_dpu_trd DPU

Write sd_card.img to SD card using SD card reader.

The **sd_card.img** file is output of the compilation and packing by Vitis. It is located in directory:

~/work/te0820_84_240/test_board_dpu_trd/dpu_trd_system/Hardware/package

In Windows 10 (or Windows 11) PC, inst all program **Win32DiskImager** for this task. Win32 Disk Imager can write raw disk image to removable devices. https://win32diskimager.org/

Boot the board and open terminal on the board either by connecting serial console connection, or by opening ethernet connection to ssh server on the board, or by opening terminal directly using window manager on board. Continue using the embedded board terminal.



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Detailed guide how to run embedded board and connect to it can be found in <u>Run Compiled</u> <u>Example Application for Vector Addition</u>.

7.1 Resize EXT4 Partition

Check ext4 partition size by:

| root@Trenz:~# | cd | / | | | | | | |
|---------------|----|---|-----------|--------|-----------|------|---------|----|
| root@Trenz:~# | df | • | | | | | | |
| Filesystem | | | 1K-blocks | Used | Available | Use% | Mounted | on |
| /dev/root | | | 564048 | 398340 | 122364 | 77% | / | |

Resize partition

```
root@Trenz:~# resize-part /dev/mmcblk0p2
```

Check ext4 partition size again, you should see:

| root@Trenz:~# dfh | | | | | | |
|-------------------|------|--------|-----------|------|---------|----|
| Filesystem | Size | Used | Available | Use% | Mounted | on |
| /dev/root | 6.1G | 390.8M | 5.4G | 7% | / | |

The available size would be different according to your SD card size.

Set DISPLAY variable:

root@petalinux:~# export DISPLAY=:0.0

Set path to Xilinx Firmware:

```
root@petalinux:~# export
XLNX VART FIRMWARE=/run/media/mmcblk1p1/dpu.xclbin
```

7.2 Test the Integrated DPUCZDX8G

For both tested modules, the integrated DPU can be tested by command:

```
xdputil query
```

Command and reply in case of module with ID=84 (DPU configuration B4096):



```
"regmap":"1to1 version"
    },
    "VAI Version":{
        "libvart-runner.so":"Xilinx vart-runner Version: 3.0.0-
c5d2bd43d951c174185d728b8e5bcda3869e0b39 2023-08-27-07:37:08 ",
        "libvitis ai library-dpu task.so":"Xilinx vitis ai library
dpu task Version: 3.0.0-c5d2bd43d951c174185d728b8e5bcda3869e0b39 2023-
01-13 06:58:30 [UTC] ",
        "libxir.so":"Xilinx xir Version: xir-
c5d2bd43d951c174185d728b8e5bcda3869e0b39 2023-08-27-07:36:08",
        "target factory":"target-factory.3.0.0
c5d2bd43d951c174185d728b8e5bcda3869e0b39"
    },
    "kernels":[
        {
            "DPU Arch": "DPUCZDX8G ISA1 B4096",
            "DPU Frequency (MHz)":300,
            "IP Type":"DPU",
            "Load Parallel":2,
            "Load augmentation": "enable",
            "Load minus mean":"disable",
            "Save Parallel":2,
            "XRT Frequency (MHz)":300,
            "cu addr":"0xa0010000",
            "cu handle":"0xaaab00c1b120",
            "cu idx":0,
            "cu mask":1,
            "cu name":"DPUCZDX8G:DPUCZDX8G 1",
            "device id":0,
            "fingerprint":"0x101000056010407",
            "name":"DPU Core 0"
        }
    ]
}
root@trenz:~#
```

Command and reply in case of module with ID=106 (DPU configuration B1024):

| signar p | | | https://sp.utia.cas.cz |
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```
root@trenz:~# xdputil query
{
    "DPU IP Spec":{
        "DPU Core Count":1,
        "IP version":"v4.1.0",
        "generation timestamp":"2023-02-21 21-30-00",
        "git commit id":"7d32c41",
        "git commit time":2023022121,
        "regmap":"1to1 version"
    },
    "VAI Version":{
        "libvart-runner.so":"Xilinx vart-runner Version: 3.0.0-
c5d2bd43d951c174185d728b8e5bcda3869e0b39 2024-01-18-07:15:08 ",
        "libvitis ai library-dpu task.so":"Xilinx vitis ai library
dpu task Version: 3.0.0-c5d2bd43d951c174185d728b8e5bcda3869e0b39 2023-
01-13 06:58:30 [UTC] ",
        "libxir.so":"Xilinx xir Version: xir-
c5d2bd43d951c174185d728b8e5bcda3869e0b39 2024-01-18-07:13:09",
        "target factory":"target-factory.3.0.0
c5d2bd43d951c174185d728b8e5bcda3869e0b39"
    },
    "kernels":[
        {
            "DPU Arch": "DPUCZDX8G ISA1 B1024",
            "DPU Frequency (MHz)":300,
            "IP Type":"DPU",
            "Load Parallel":2,
            "Load augmentation": "enable",
            "Load minus mean":"disable",
            "Save Parallel":2,
            "XRT Frequency (MHz)":300,
            "cu addr":"0xa0010000",
            "cu handle":"0xaaab02346ca0",
            "cu idx":0,
            "cu mask":1,
            "cu name": "DPUCZDX8G: DPUCZDX8G 1",
            "device id":0,
```



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7.3 Remote Monitoring and Configuration Support

The configured OS includes work in progress version of a remote monitoring and configuration support server. It can be used for remote reading of content of the SD card partition mmcblk0p1.

Button Reboot device can be used for system reboot. Ethernet connection is lost, but remote PC www browser remains open and waits for possible reconnection.

| 20_04_Viti | s_2022_2_Petalinux_te0802_2cg_1eg_1gb_vga - VMware Workstation 16 Player | | | - | - 🗆 × |
|------------------|---|---|----|------------|-------|
| <u>P</u> layer ▼ | - 4 □ 2 | | | | « 📄 |
| Activities | 👌 Firefox Web Browser 👻 | Jan 3 08:20 • | | . ● | () ▼ |
| | Trenz Module Monitoring an × + | ~ | | - 0 | 8 |
| | $\leftarrow \rightarrow C$ \bigcirc \geqq 192.168.13.162 | ជ | | گ | = |
| | Trenz Module Monitorir | ng and Configuration - work in proces | ss | | |
| Â | SD card QSPI flash electronic | | | | |
| ? | Reboot system | Content of the SD card (mmcblk0p1): | 1 | | |
| | Reboot device | total 32M -rwxrwx 1 root disk 5.8M Jan 1 2015 BOOT.BIN -rwxrwx 1 root disk 21M Jan 1 2015 Image -rwxrwx 1 root disk 2.8K Jan 1 2015 boot.scr -rwxrwx 1 root disk 4.2M Jan 1 2015 dpu.xclbin -rwxrwx 1 root disk 4.2M Jan 1 2015 fpu.xclbin -rwxrwx 1 root disk 295 Jan 1 2015 fpu.rcbin -rwxrwx 1 root disk 4.2M Jan 1 2015 fpu.rcbin -rwxrwx 1 root disk 295 Jan 1 2015 fpu.rcbin -rwxrwx 1 root disk 2015 dpu.rcbin -rwxrwx | | | |
| | Read operation | -rwxrwx 1 root disk 43x Jan 1 2015 system.utb -rwxrwx 1 root disk 58M Jan 1 2015 sest dpu_trd -rwxrwx 1 root disk 39K Dec 8 12:49 vga.elf | | | |
| | Read SD0 Read SD1 | Done | | | |
| | Write operation | | | | |
| | SD0: Browse No file selected. Write mmcblk0p1 | | | | |
| | SD1: Browse No file selected. Write mmcblk1p1 | | | | |
| | Web interface is for general usage, check which mmcblk*p1 is available on your device | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

After reboot of the evaluation board, the network DHCP server assigns Ethernet address to the evaluation board.

If the network DHCP address assignment algorithm assigns the identical Ethernet address, the page can be refreshed and the connection is re-established again.



If the network DHCP address assignment algorithm assigns different Ethernet address, the connection has to be established on the new Ethernet address.

7.4 Remote Control from Ubuntu X11 Desktop.

The configured OS also supports X11 desktop on remote PC via Ethernet. In remote PC in Ubuntu OS, in PuTTY terminal utility with ssh Ethernet connection to the board with enabled X11 forwarding.

Openning.

Log in to the evaluation board as user root with pswd root

Start two rxvt terminal emulators by typing in PuTTY terminal:

rxvt &

rxvt &

In first rxvt terminal emulator window start utility

top

In second rxvt terminal emulator start

mc

You can see two applications running on the evaluation board with output on the remote desktop. Remote PC kbd and mouse are used for control of these applications.



Closing.

On remote PC, close top utility by Ctrl-C. Stop mc utility by F10.

Close open terminal emulators by typing exit or by mouse click on x icon in the right top corner of terminal emulator window. Close PuTTY connection by typing exit or by mouse click on x icon in the right top corner of PuTTY window.

7.5 Remote Control in x-session-manager on Ubuntu X11 Desktop.

The configured OS also supports x-session-manager on X11 desktop on remote PC connected via Ethernet to the evaluation board.

Opening.

In remote PC in Ubuntu OS, start PuTTY terminal utility with ssh Ethernet connection to the board with enabled X11 forwarding.





Log in to the evaluation board as user root with pswd root In PuTTY terminal, start x-session-manager by typing:

x-session-manager &

The desktop (displayed on the VGA display of the evaluation board) is also displayed in the remote PC X11 desktop. Start two rxvt terminal emulators by typing in PuTTY terminal:

rxvt & rxvt &

In first rxvt terminal emulator window start utility top In second rxvt terminal emulator start mc

You can see two applications running on the evaluation board with output on the remote desktop. Remote PC kbd and mouse are used for control of these applications.



Closing.

On remote PC, close top utility by Ctrl-C. Stop mc utility by key F10.

Close open terminal emulators by typing exit or by mouse click on x icon in the right top corner of terminal emulator window. Close PuTTY connection by typing exit or by mouse click on x icon in the right top corner of PuTTY window.

7.6 Display Test Pattern and Test USB Camera

Complete video chain can be tested with output to the X11 desktop.

To display the test pattern, use this gstreamer command:

gst-launch-1.0 videotestsrc ! ximagesink

To display USB camera video, use this gstreamer command:

signal processing

https://sp.utia.cas.cz



gst-launch-1.0 v4l2src device=/dev/video0 ! videoconvert ! ximagesink

Video output is directed to the local HD VGA display, if the command is started from local X11 console.

Video output is directed to the remote X11desktop, if the command is started from the remote X11 console.



Test pattern is displayed on remote PC X11 desktop

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Full HD video from USB camera is displayed as Full HD on remote PC X11 desktop.



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7.7 Vitis AI 3.0 TE-4EV-1E-2GB Module ID=84, TE0701-06, DPU (B4096)

| Vitis AI 3.0 exampes | Perfor | Power | Perfor | Power | GigaOp |
|---|--------|-------|--------|--------|--------|
| | manc | with | mance | with | S |
| | e with | camer | input | input | input |
| | input | a and | from | from | from |
| | from | VGA | file | file | file |
| | camer | [W] | e2e | e2e | e2e |
| | a e2e | | (-t 3) | (-t 3) | (-t 3) |
| | [FPS] | | [FPS] | [W] | [Gops] |
| Face detection Model: pt_face-mask- | 30.0 | 10.0 | 113 | 9.8 | 75.7 |
| detection_512_512_0.67G_3.0 | | | | | |
| Vehicle make Model: pt_vehicle-make- | 30.0 | 10.5 | 167 | 13.6 | 607.9 |
| classification_VMMR_224_224_3.64G_3.0 | | | | | |
| Vehicle type Model: pt_vehicle-type- | 30.0 | 10.5 | 167 | 13.6 | 607.9 |
| classification_CarBodyStyle_224_224_3.64G_3.0 | | | | | |
| Vehicle color Model: pt_vehicle-color- | 30.0 | 10.5 | 167 | 13.6 | 607.9 |
| classification_VCoR_224_224_3.64G_3.0 | | | | | |
| General classification Model: | 30.0 | 11.9 | 59.6 | 13.0 | 488.7 |
| pt_resnet50_imagenet_224_224_8.2G_3.0 | | | | | |
| General classification Model: | 30.0 | 11.5 | 69.2 | 12.7 | 401.3 |
| pt_resnet50_imagenet_224_224_0.3_5.8G_3.0 | | | | | |
| General classification Model: | 30.0 | 11.2 | 73.8 | 12.4 | 361.6 |
| pt_resnet50_imagenet_224_224_0.4_4.9G_3.0 | | | | | |
| General classification Model: | 30.0 | 11.0 | 81.1 | 12.2 | 332.5 |
| pt_resnet50_imagenet_224_224_0.5_4.1G_3.0 | | | | | |
| General classification Model: | 30.0 | 10.7 | 91.1 | 11.9 | 300.6 |
| pt_resnet50_imagenet_224_224_0.6_3.3G_3.0 | | | | | |
| General classification Model: | 30.0 | 10.6 | 99.6 | 11.5 | 249.0 |
| pt_resnet50_imagenet_224_224_0.7_2.5G_3.0 | | | | | |

Measurement conditions:

- TE0820-03-04EV-1EA 2GB module with 12V FAN on TE0701-06 carrier board
- DPU in B4096 configuration
- USB WWW colour camera logi 720p, Logitech, 1280x720p30, 30 FPS
- Remote X11 desktop
- Power supply 12V/5A •
- Power measured at the 230V power plug



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7.8 Vitis AI 3.0 TE0820-05-2AE21MA module ID=106, TE0707-02, DPU (B1024)

| Vitis AI 3.0 exampes | Perfor | Power | Perfor | Power | GigaOp |
|---|--------|-------|--------|--------|--------|
| | manc | with | mance | with | S |
| | e with | camer | input | input | input |
| | input | a and | from | from | from |
| | from | VGA | file | file | file |
| | camer | [W] | e2e | e2e | e2e |
| | a e2e | | (-t 3) | (-t 3) | (-t 3) |
| | [FPS] | | [FPS] | [W] | [Gops] |
| Yolov4 face mask detection Model: pt_face- | 20.0 | 6.6 | 58.5 | 6.1 | 39.2 |
| mask-detection_512_512_0.67G_3.0 | | •••• | •••• | •••• | |
| Vehicleclassification vehicle make Model: | 20.0 | 6.8 | 43.7 | 6.7 | 157.3 |
| pt_vehicle-make- | | | - | | |
| classification_VMMR_224_224_3.64G_3.0 | | | | | |
| Vehicleclassification vehicle type Model: | 20.0 | 6.8 | 43.7 | 6.7 | 157.3 |
| pt_vehicle-type- | | | | | |
| classification_CarBodyStyle_224_224_3.64G_3.0 | | | | | |
| Classification vehicle color Model: pt_vehicle- | 20.0 | 6.8 | 43.7 | 6.7 | 157.3 |
| color-classification_VCoR_224_224_3.64G_3.0 | | | | | |
| Classification Model: | 18.2 | 7.5 | 19.1 | 6.8 | 156.6 |
| pt_resnet50_imagenet_224_224_8.2G_3.0 | | | | | |
| Classification Model: | 20.0 | 7.2 | 24.8 | 6.8 | 143.8 |
| pt_resnet50_imagenet_224_224_0.3_5.8G_3.0 | | | | | |
| Classification Model: | 20.0 | 7.1 | 28.1 | 6.8 | 137.7 |
| pt_resnet50_imagenet_224_224_0.4_4.9G_3.0 | | | | | |
| Classification Model: | 20.0 | 7.0 | 32.0 | 6.8 | 131.2 |
| pt_resnet50_imagenet_224_224_0.5_4.1G_3.0 | | _ | | | _ |
| Classification Model: | 20.0 | 6.9 | 37.3 | 6.8 | 123.1 |
| pt_resnet50_imagenet_224_224_0.6_3.3G_3.0 | | | | | |
| Classification Model: | 20.0 | 6.8 | 44.0 | 6.8 | 110.0 |
| pt_resnet50_imagenet_224_224_0.7_2.5G_3.0 | | | - | | |

Measurement conditions:

• TE0820-05-2AE21MA module (2CG-1E device, 2GB DDR4), TE0707 carrier board

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- DPU in B1024 configuration
- USB WWW camera ETERNICO ET201 Full HD, sensor JX_F23, 1920x1080, 20 FPS
- Remote X11 desktop
- Power supply 5V/4A
- Power measured at the 230V power plug





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This application and evaluation package will be based on the STM32CubeH5 Firmware Examples for STM32H5xx Series Application based on NetXDuo: **Nx_WebServer.** This STM application provides an example of Azure RTOS NetX Duo stack usage on STM32H573G-DK board, it shows how to develop Web HTTP server based application. <u>https://htmlpreview.github.io/?https://raw.githubusercontent.com/STMicroelectronics/STM 32CubeH5/master/Projects/STM32CubeProjectsList.html</u>

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https://zs.utia.cas.cz/index.php?ids=projects/eecone

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TE0802-02-1AEV2-A test board Vitis AI Tutorial (Vitis 2021.2.1, Vitis AI 2.0, no VGA display support) <u>https://wiki.trenz-electronic.de/display/PD/TE0802-02-1AEV2-</u> <u>A+test+board+Vitis+AI+Tutorial</u>

[9]



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TE0802-02-1AEV2-A test board Vitis AI Tutorial

(Vitis 2021.2.1, Vitis AI 2.0, no VGA display support) https://wiki.trenz-electronic.de/display/PD/TE0802-02-1AEV2-A+test+board+Vitis+AI+Tutorial

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MPSoC Development Board with AMD Zynq[™] UltraScale+[™] ZU2CG and 1 GB LPDDR4, Trenz Electronic.

https://shop.trenz-electronic.de/en/TE0802-02-1BEV2-A-MPSoC-Development-Boardwith-AMD-Zyng-UltraScale-ZU2CG-and-1-GB-LPDDR4?c=474

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TE0821 Resources, TE0821 - 4 x 5 cm SoC module with Xilinx Zynq UltraScale+, prepared and published by Trenz Electronics

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TE0820 test board Vitis AI 3.0 Tutorial, v25, has been prepared by UTIA (before EECONE start) for Trenz Electronics and it has been published by Trenz Electronics 31.8.2023.

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