PRESS RELEASE

A NEW EUROPEAN PROJECT:

DYNAMICALLY RECONFIGURABLE SYSTEM DESIGN METHODOLOGY

DEVELOPMENT INITIATED BY A USERS AND MANUFACTURERS CONSORTIUM WITH THE SUPPORT OF THE EUROPEAN COMMISSION IN THE FRAME OF THE IST PROGRAMME

Named RECONF, its aim is to develop the required design environment to be able to efficiently use dynamically reconfigurable FPGAs (D_FPGAs).

The technology will open new application opportunities, will make possible to design innovative low cost architectures, for adaptive computing systems having to adapt permanently their algorithms to their changing environment.

The main targeted application domains are: real time image processing, signal processing,... included in most of embedded systems, e.g. in aerospace, automotive, multimedia, industrial process control.

Although the environment will be usable by all Real Time embedded systems manufacturers, it will be a unique opportunity for SMEs to access this new technology and to develop complex, high performance applications at low costs.

THE PROBLEM STATEMENT

Future systems will get more and more complex in terms of computing requirements.
Some processing algorithms need to be implemented in Hardware (ASIC, FPGA) rather than Software (DSP, processors) for performance issues (inherent parallelism allows achievable operating frequencies, especially for video applications; lower power consumption).

FPGA is a good complementary technology to the ASIC one. However, large FPGA devices are characterised by high production costs (average ratio: 5 to 10), higher power consumption (average ratio: 10 compared to ASIC) and may not be large enough for some complex applications (video for instance).

D_FPGAs are becoming available on the market, alleviating most of the above drawbacks, by offering real new opportunities.

Complex applications can be broken up into several modules that can be processed sequentially by dynamically re-configuring the FPGA, allowing the use of smaller and cheaper devices.

The application can re-configure a subset of the FPGA while the rest of the device keeps operating.

Thanks to the possibility to use smaller FPGA matrices because of the re-configurability, many benefits can be expected for the products: less power consumption, better reliability, lower production cost, lower radiation susceptibility, etc; all being drawbacks of classical FPGAs.

So what is the problem of using this rather new D_FPGA technology?

Even if Silicon parts are becoming available on the market, there are no adapted design methodologies and no tools on the market to support electronic designs based D_FPGAs. Developments are still using classical design environments, which are not adapted to an efficient approach, especially regarding the dynamic system specificity.

OUTPUTS OF THE PROJECT

The aim of this project is to allow implementation of adaptive system architectures by defining an adapted Methodology and developing the required Design Environment to be able to take full benefits of D_FPGA.

The outputs of the RECONF project will be a complete and validated design environment:

- New and adapted design methodology addressing partitioning, scheduling issues…: Availability of a Guide. As a very original output from RECONF, and part of the dissemination effort, this guide will be made widely available for free.
- Adapted to D_FPGAs and validated front end tools
- Adapted to D_FPGAs and validated back end tools

The first point is technology independent as probably the second point is, and will be re-usable for any D_FPGA families. Back end tools are linked to the targeted FPGA family and will be applied to the D_FPGA family available today on the market from the Consortium semiconductor manufacturer.

This environment will be fully validated through complementary industrial evaluations organised in order to cover:

- data management during reconfiguration and test & debug
- states machine;
- complex algorithms & real time aspects.

THE COVERED ISSUES

The problems that will be addressed are:

- Technical issues

  Duration of the re-configuration phase: To be reduced as much as possible for real time applications.

  Per block re-configuration: Real time applications (loop control…) are not compatible with processes to be stopped Partial re-configuration of the FPGA on a per-block basis is necessary. This emphasises an IP approach.

  Management of internal data: Processes may have different life phases, with some algorithm changes in each of them. Coupled with the previous point, the data used and produced by calculations need to be preserved while making partial re-configurations.

- Methodology and tools issues

  "Classical" design environments are based on a functional approach. Timing issues are respected at a late stage of the design. It is to be changed, as it is necessary to consider *functional* block timings. It is of high importance to know very early in the development what resources will be associated with a specific function and when they will be activated.

  Dynamic re-configuration management: The way to chain / sequence re-configurations is a difficult task. This issue can be addressed either by software executed on an additional embedded processor (but at a cost), or using tools coupled with the ones used for FPGA design and able to generate states machines.

  Test and debug issues: Complex dedicated circuits are painful and time consuming to test & debug. Adding a new feature such as re-configurability will emphasises this issue. Additional debug means are an absolute necessity.

PROJECT PLANNING AND TIMETABLE

The project is scheduled over 31 months. The duration of each of the four main activities will be:

1. Methodology: over 20 months
2. Technology / Tools development: over 23 months
3. Evaluation, validation: over 18 months
4. Dissemination / Implementation: over 31 months

THE MEMBERS OF THE CONSORTIUM

A special effort has been spent to form a well-balanced Consortium to cover all the objectives of the project. It involved 6 partners from 5 European countries:

- 1 Semiconductor Manufacturer – Atmel – supporting the Tools to give to the consortium access to its D_FPGA technology.
- 2 partners for methodology and front end tools development: UPC, UTIA. They both are deeply involved in FPGA technology. As academics, they will bring the consortium with the latest ideas and techniques to fulfil the project objectives.
- 3 Industrial End Users: Deltatec, Kayser Italia, MBDA France (Consortium Leader). To validate the Methodology and Design Environment with 3 different application fields: Aeronautic, Space, Multimedia to validate the complementary aspects

About Atmel

Founded in 1984, Atmel Corporation is headquartered in San Jose, California with manufacturing facilities in North America and Europe. Atmel designs, manufactures and markets worldwide, advanced logic, mixed-signal, nonvolatile memory and RF semiconductors. Atmel is also a leading provider of system-level integration semiconductor solutions using CMOS, BiCMOS, SiGe, and high-voltage BCDMOS process technologies.

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About DELTATEC

DELTATEC (Ans, BELGIUM) provides advanced electronic hardware and software design services. Competence centres such as FPGA, DSP and Win CE represent the different technologies mastered by DELTATEC and its ability to develop complex projects.

DELTATEC designs FPGAs, dedicated boards and multi-board systems from concept to product with a strong focus on digital imaging applications: broadcast video, image distribution, image processing, image synthesis.

www.deltatec.be

About Kayser Italia (KI)

KI is a private Italian company, established in 1986. The company is actively working in the study, design, manufacturing, integration and testing of systems and subsystems for advanced industrial research and space applications. These applications require outstanding performances in a severe environment, with an high level of integration, low power consumption, and the mechanical interfaces impose hard constraints. KI participated to the development of 12 payloads, and to 19 space missions, both on Russian Satellites and Shuttle.

The company has a staff of 30 persons, with experience in electronics, computer science, physics, optics and mechanics, allowing to operate both as sub-contractor and prime-contractor for the European and Italian Space Agencies (ESA and ASI).

KI is certified ISO9001, certification to ESA PSS standards for personnel manufacturing PCBs and harness and for P.A. Inspector is maintained regularly.

www.kayser.it

About MBDA

MBDA is Europe's leading guided weapons group with 45 missile systems in operational service and a further 30 in development for air forces, armies and navies around the world. The Company has a strategic interest in the development of highly performant and integrated embedded real time computers.

The group employs 10,000 across 12 main sites in Europe and the USA and is jointly owned by BAE SYSTEMS (37.5%), EADS (37.5%) and Finmeccanica (25%).

MBDA France is leading the RECONF Consortium.

www.mbda.fr

About UPC, Universitat Politecnica De Catalunya

UPC is one of the main technical universities in Spain, with more than 30.000 students, 15 schools, 40 departments and around 2500 people involved in teaching and research activities. The Advanced Hardware Architectures (AHA) team belongs to the Electronic Engineering Department of UPC. The staff (12 people) of the AHA team has experience in electronic system design (analogue and digital), high level description and synthesis of electronic systems, with specific competences in the design of FPGA architectures and FPGA-based design of embedded systems. Research topics of the AHA team include also soft computing models (fuzzy models, artificial neural networks), as well as bio-inspired systems.

www-eel.upc.es/aha/

About UTIA

The Institute of Information Theory and Automation (UTIA) is a research institute of the Academy of Sciences of the Czech Republic. It is concerned with the development of control, information and computer sciences including in particular system theory, data processing and random processes from the point of view of mathematical modelling, decision-making, automatic control and signal processing. The research staff, of 80 researchers, covers a wide range of scientific areas, from the advanced parts of theoretical and applied mathematics to the sophisticated aspects of computer programming and advanced engineering applications.

www.utia.cas.cz/ZS